Chapter 10

New Tools for the Direct Characterisation of FinFETS

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10.1 Introduction

This chapter discusses how classical transport theories such as the thermionic emission (Sze, 1981), can be used as a powerful tool for the study and the understanding of the most complex mechanisms of transport in fin field effect transistors (FinFETs). By means of simple current and differential conductance measurements, taken at different temperatures and different gate voltages (V_G's), it is possible to extrapolate the evolution of two important parameters such as the spatial region of transport and the height of thermionic barrier at the centre of the channel. Furthermore, if the measurements are used in

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conjunction with simulated data, it becomes possible to also extract the interface trap density of these objects. These are important results, also because these parameters are extracted directly on state-of-the-art devices and not in specially designed test structures. The possible characterization of the different regimes of transport that can arise in these ultra-scaled devices having a doped or an undoped channel are also discussed. Examples of these regimes are full body inversion and weak body inversion. Specific cases demonstrating the strength of the thermionic tool are discussed in Sections 10.2, 10.3, and 10.4.

10.2 Transport in Doped N-FinFETs

Non-planar field-effect transistors called FinFETs (Hisamo *et al.*, 2000) have been developed to solve the issues of gate control encountered with the standard planar geometry when the channel length is reduced to a sub-45 nm size. Their triple-gate geometry is expected to have a more efficient gate action on the channel and to solve the leakage problem through the body of the transistor, one of the most dramatic short channel effects (Hisamo *et al.*, 2000). However, their truly three-dimensional (3D) structure makes doping — and thus also potential — profiles very difficult to simulate and to understand using previous knowledge on device technology. Transport studies at low temperature, where the thermally activated transport is suppressed, can bring insight to these questions by measuring local gate action. For these reasons, in a recent work (Sellier *et al.*, 2007), the potential profile of these devices has been investigated by conductance measurements. This has allowed the observation of the formation of a sub-threshold channel at the edge of the silicon nanowire. This corner effect has been proposed (Doyle *et al.*, 2003; Fossum *et al.*, 2003) as an additional contribution to the sub-threshold current in these 3D triple-gate structures, where the edges of the nanowire experience stronger gate action due to the geometric enhancement of the electric field. However, besides extensive simulation work (Doyle *et al.*, 2003; Fossum *et al.*, 2003) — due to the difficulties with these 3D structures — very little experimental work (Xiong *et al.*, 2004) has been published previous

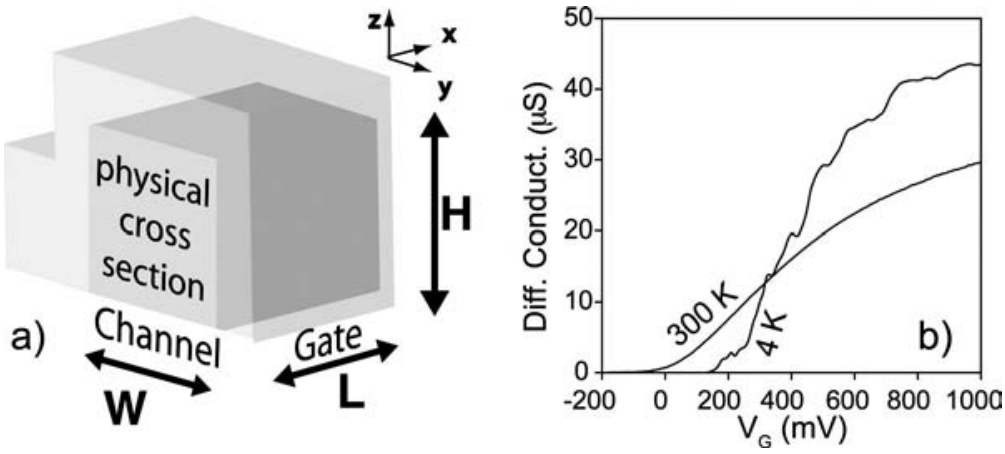

Figure 10.1. (a) Schematic of the FinFET geometry where the gate surrounds the Si nanowire (the fin). (b) Low Bias differential conductance vs. gate voltage for a long and narrow silicon FinFET ($L = 950$ nm, $W = 35$ nm).

to the ones discussed in this chapter. This paragraph focusses on the description of the experimental observation of the corner effect on doped devices identical to the ones described in the next chapter (see Fig. 10.1a).

10.2.1 *Thermionic Emission in Doped FinFET Devices*

The aim of this section is to show that, by using a combination of differential conductance ($G = dI_{SD}/dV_{SD}$) versus V_G traces taken at different temperature, and of low temperature Coulomb blockade (CB) (see Sellier *et al.* (2007) and references therein) measurements, it is possible to infer the existence of a dot located at the edge of the fin and thus of the corner effect (Doyle *et al.*, 2003; Fossum *et al.*, 2003).

In the investigated device series the height of the fin wire is always $H = 65$ nm, while the width ranges from $W = 35$ nm to 1 μm and the gate length ranges from $L = 50$ nm to 1 μm. The relatively high p-type doping ($\sim 10^{18}$ cm^{-3}) of the channel wire is chosen to ensure a depletion length shorter than half the channel length in order to have a fully developed potential barrier in this n-p-n structure and so to keep the conductance threshold at a large enough positive gate voltage. The characteristics at room temperature of these nanoscale FinFETs look therefore similar to

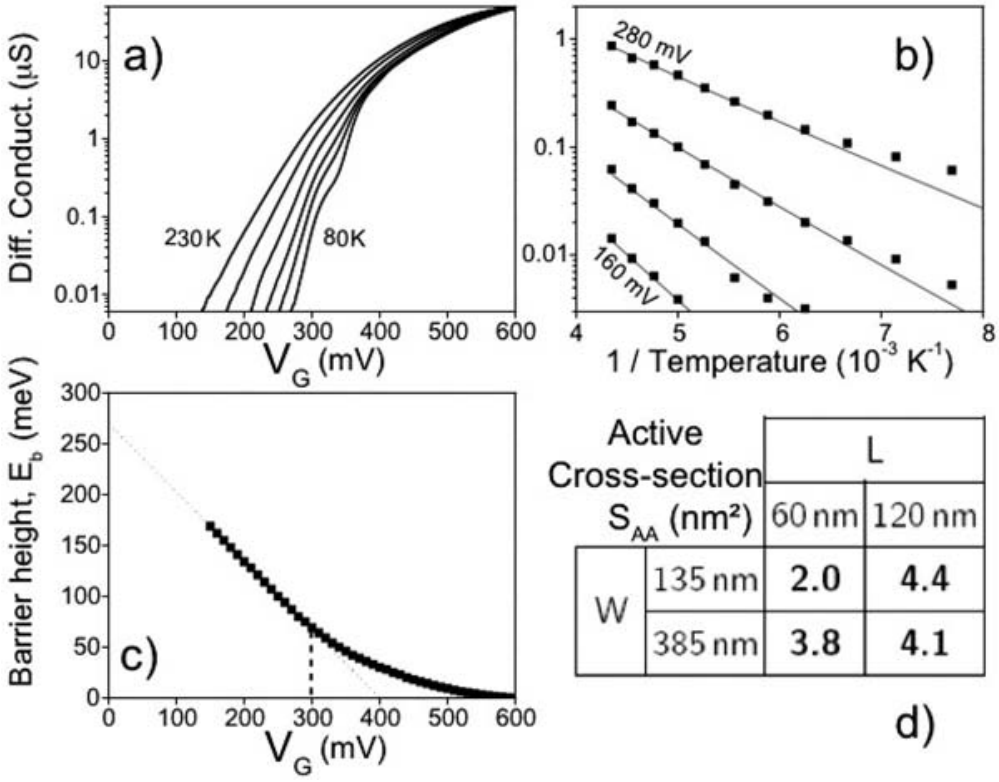

Figure 10.2. (a) Differential conductance vs gate voltage for a short and wide fin ($L = 60$ nm, $W = 385$ nm). (b) Differential conductance plotted vs the inverse of the temperature for the same sample. The conductance is thermally activated above 150 K. (c) Barrier height vs V_G changing behavior at 300 mV (same sample). (d) Measured cross section S_{AA} for the activated current of 4 samples with different lengths L and widths W.

those of their larger planar counterparts (see Fig. 10.1b at 300 K). For sub-threshold voltages, a thermionic barrier (E_b) (Sze, 1981) exists between the source and drain electron reservoirs and the transport is thermally activated at high enough temperature, as shown in Fig. 10.2a,b. For very short devices, G is simply given by the thermionic emission above the barrier according to the formula (Sze, 1981):

$$G_{3D} = S_{AA} A^* T \frac{e}{k_B} exp\left(-\frac{E_b(V_G)}{k_B T}\right) \qquad (10.1)$$

where the effective Richardson constant A^* for Si is 2.1× 120 A cm^2 K^2, T is the temperature, k_B the Boltzmann constant, e the elementary charge and S_{AA} represents the active cross section, which can be interpreted as a good estimation of the portion

of the physical cross section area through which the transport preferentially occurs (Sze, 1981).

10.2.2 *Analysis of the Thermionic Regime (High Temperatures)*

Several samples have been measured in this thermionic regime (80 K $\leqslant T \leqslant$ 250 K) and their conductance has been fitted using Eq. (10.1) to obtain E_b and S_{AA} (see Fig. 10.2c,d). The two 385 nm wide samples have the same cross section $S_{AA} \approx 4$ nm^2 although their length differ by a factor of 2. It is therefore possible to conclude that, in the sub-threshold regime transport is dominated by thermionic emission in these devices. The two 135 nm-wide samples, however, have different S_{AA} values, but this cannot imply a diffusive transport since the longest sample has the largest conductance. Another result is that the cross section $S_{AA} \approx 4$ nm^2 is much smaller than the channel width W (135 or 385 nm) multiplied by the channel interface thickness (about 1 nm). This result is consistent with the corner effect that produces a lower conduction band (stronger electric field) along the two edges of the wire, where the current will flow preferentially (Fig. 10.3b). The barrier height E_b versus gate voltage is plotted in Fig. 10.2c. The data extrapolated to zero gate voltage are consistent with a 220 meV barrier height calculated for a p-type channel in contact with a n++ gate through a 1.4 nm SiO_2 dielectric (Sze, 1981). The linear dependence of the barrier height shows a good channel/gate coupling ratio, $\alpha = dE_b/(dV_G) = 0.68$, due to the triple-gate geometry with a thin gate oxide. At higher gate voltage (above 300 mV), the coupling ratio decreases and a finite barrier survives up to large voltages.

10.2.3 *Analysis of the Coulomb Blockade Regime (Low Temperatures)*

Analysis of the low-temperature transport (4 K $\leqslant T \leqslant$ 60 K, see below) shows that the gate action remains constant inside the channel where localised states are formed. Two confining barriers are formed in the access regions (between channel and contacts), where the concentration of implanted arsenic atoms is

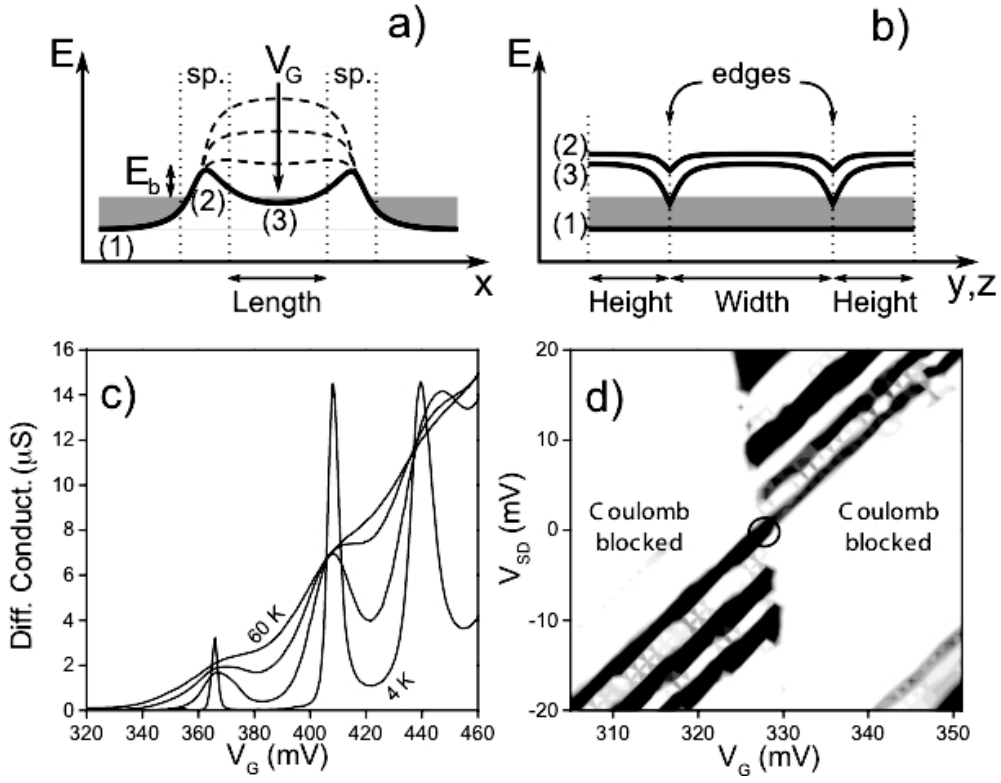

Figure 10.3. (a) Conduction band edge profile with the highest barrier in the channel or in the access regions below the spacers (sp.) depending on the gate voltage. (b) Band edge along the gate oxide interface (1) in the contacts, (2) in the barriers, and (3) in the channel. The corner effect produces two channels with low barriers at the wire edges. (c) Differential conductance vs gate voltage for a short and wide channel ($L = 60$ nm, $W = 385$ nm) showing Coulomb blockade peaks up to high temperatures (20 K steps). (d) Stability diagram, i.e., conductance vs gate and bias voltages at 4.2 K. The circle indicates a zero bias conductance peak, which develops into a triangular sector at finite bias.

reduced by the masking silicon nitride spacers placed next to the gate (see Fig. 10.3a). For long channels and at low temperatures the conductance develops fluctuations versus gate voltage (see Fig. 10.1b) with a pattern that reproduces after thermal cycling (at least for the main features). These fluctuations are caused by quantum interferences in the channel. For gate voltages close to the threshold, charge localization occurs, especially for short fins. In fact, when short channel devices are cooled down to 4.2 K, conductance pattern develops a series of peaks, as can be seen in Fig. 10.3c, that can be attributed to Coulomb blockade of electrons in the potential

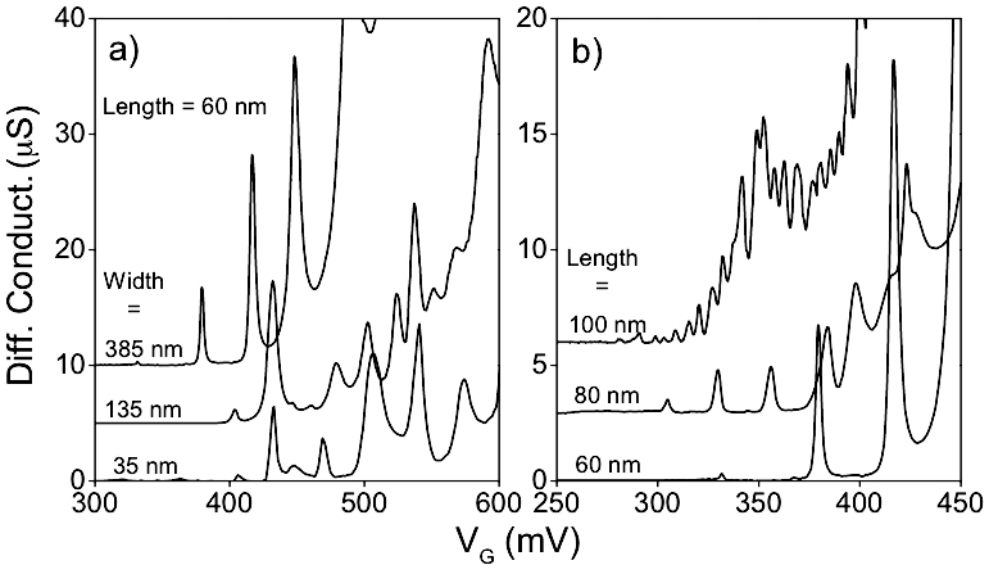

Figure 10.4. Differential conductance vs V_G at 4.2 K for several devices. (a) Short fins ($L = 60$ nm) of different widths ($W = 35, 135, 385$ nm) have a similar peak spacing. (b) Devices with longer fins ($L = 60, 80, 100$ nm) have a smaller peak spacing (the widths are different). The curves have been shifted for clarity.

well created in the channel by the two tunnel barriers of the low-doped access regions (Sellier *et al.*, 2007). This interpretation is supported by the channel-length dependence of the peak spacing discussed later. An explanation in terms of a quantum well formed by an impurity can be ruled out. An impurity or defect could not accept many electrons, i.e., more than 20 for the 100 nm sample in Fig. 10.4b, since they represent a single charge or empty state.

10.2.4 *Interpretation of the Results*

These results can be interpreted as follows: Devices with shorter channel act as quantum dots where the conduction electrons are spatially localised and are Coulomb blockade for the transport by a finite charging energy bias. In the stability diagram of a quantum dot (see Fig. 10.3d), the slopes of a triangular conducting sector give the ratios of the capacitances C_G, C_S, and C_D between the dot and, respectively, the gate, source, and drain electrodes. In this way the dot/gate coupling $\alpha = C_G/(C_G + C_S + C_D) = 0.78$ (0.65) for the first (second) resonance is found. These values are close to the

channel/gate coupling of 0.68 obtained independently in the same sample from the gate voltage dependence of the barrier height in the middle of the channel at higher temperatures. This result indicates that the gate coupling in the centre of the device remains constant and supports the idea of a minimum in the conduction band, as sketched in (Fig. 10.3b). The peak spacing, ΔV_G, is the change in gate voltage that increases by 1 the number of electrons in the dot located at the silicon/oxide interface. This quantity provides the dot/gate capacitance $C_G = e/\Delta V_G$, and then the dot area $S = C_G/C_{ox}$ using the gate capacitance per unit area $C_{ox} = \epsilon_{ox}/t_{ox} = 0.025$ F/m^2. The peak spacings for the same gate length ($L = 60$ nm) but three different channel widths ($W = 35$, 135, and 385 nm) can be compared in Fig. 10.4a. Although the patterns are not very regular, an average peak spacing of about 30 mV is obtained for all of them, indicating similar dot areas whereas the effective width is varied by more than one order of magnitude.

10.2.5 *The Corner Effect*

The conductance patterns for three different lengths ($L = 60$, 80, and 100 nm) shown in (Fig. 10.4b) have decreasing average peak spacings ($\Delta V_G = 39$, 24, and 6 mV, respectively) and therefore increasing dot areas ($S_{AA} = 160$, 270, and 1100 nm^2). However, these areas are not strictly proportional to the gate length, so that the actual width could be length dependent or the actual dot length could be smaller than the gate length for very short fins. If it is assumed that the dot length equals the gate length, we obtain 2.7, 3.4, and 11 nm for the dot width, i.e., a small fraction of the total Si/oxide interface width $W_{eff} = W + 2H = 150$–500 nm. The observation of similar dot widths of a few nanometers for different fin widths of hundreds of nanometers is consistent with the idea of a dot located at the edge of the fin and thus with the corner effect (Doyle *et al.*, 2003; Fossum *et al.*, 2003).

10.2.6 *Temperature Dependence of the Conductance Peaks*

In addition to a large charging energy $E_c = \alpha e\Delta V_G$, these dots also have a large quantum level spacing ΔE, as can be deduced

from the temperature dependence of the conductance peaks in Fig. 10.3c. When the temperature is lowered below the level spacing, the tunneling process involves a single quantum level at a time and the peak height starts to increase above the high temperature value (Sellier *et al.*, 2007). The crossover from the classical to the quantum regime of Coulomb blockade being around 15 K, it is possible to estimate the level spacing to be about 1.3 meV. If the value $L = 60$ nm is used for the gate length, in the expression $\Delta E = 3\pi^2\hbar^2/2m^*L^2$ for the energy separation between the first and second states of a one-dimensional system, a level spacing $\Delta E = 1.6$ meV, similar to the experimental estimation, is found. This result supports the idea of a long dot extending over the whole gate length (assumed above to extract the dot width from the dot/gate capacitance).

10.2.7 *Conclusion*

In doped channel FinFETs, experiments show the existence of a few nanometers wide edge channel, which shows itself in the activated current amplitude, the Coulomb blockade peaks spacing, and the quantum levels spacing. These channels are formed along the edges the devices due to an enhanced band bending called corner effect. To utilize the full FinFET cross section for electron transport with a homogeneous current distribution, a lower sub-threshold current, and a larger on/off current ratio, this corner effect should be reduced. Better devices should have rounder corners on the scale of the depletion length and a lower doping concentration in the channel.

10.3 Transport in Undoped N-FinFETs

Section 10.2 showed that in doped FinFET the geometry and the mechanisms of sub-threshold transport are affected by the presence of screening. This screening may result in a reduction of active transistor area (i.e., corner effect) and in a sub-threshold swing (SS) degradation. Several models predicted that the introduction of an undoped channel FinFETs avoids the formation of the corner

effect (Doyle *et al.*, 2003; Fossum *et al.*, 2003) in these devices. However, it has been found that even the undoped channel devices have a non-trivial, gate voltage (V_G) dependent current distribution; there is therefore the necessity to develop tools that could be used to investigate current distribution even in these intrinsic channel devices (Tettamanzi *et al.*, 2010). Design insights could be used to improve device characteristics towards their scaling to the nanometer size regime.

10.3.1 *Introduction to Transport in Undoped Devices*

For undoped FinFETs and for widths smaller than 5 nm, full volume inversion is expected to arise (Wong (2002) and references therein). Wider devices are expected to be in the regime of weak volume inversion (where the bands in the channel closely follow the potential of V_G) only for $V_G \ll V_{th}$ (Wong, 2002; Taur, 2000). Several groups have theoretically investigated the behavior of such weak volume inversion devices using both classical (Fossum *et al.*, 2003), and quantum (Ruiz *et al.*, 2007) computational models, but no experimental method that yields information on the location of the current-carrying regions of the channel exists prior to the work discussed in this section. Taur has studied this problem analytically for an undoped channel with double gate (DG) geometry, using a 1-D Poisson equation (Taur, 2000). The main conclusion emerging from this work is that when the gate voltage is increased, a crossover takes place between the behavior of the channel at $V_G \ll V_{th}$, and at $V_G \sim V_{th}$, caused by screening of induced carriers which subsequently increase the carrier density at the gate-channel interface. This section describes the first experimental observation of this prediction, furthermore the results of a 2D model are compared with experimental data, keeping in mind that the physical principles of this are fully analogues to the 1D case of Taur.

10.3.2 *Experimental Results*

Conductance versus temperature traces for a set of eight undoped FinFET devices with the same channel length, length ($L = 40$ nm) and channel height (H $= 65$ nm) but different channel widths,

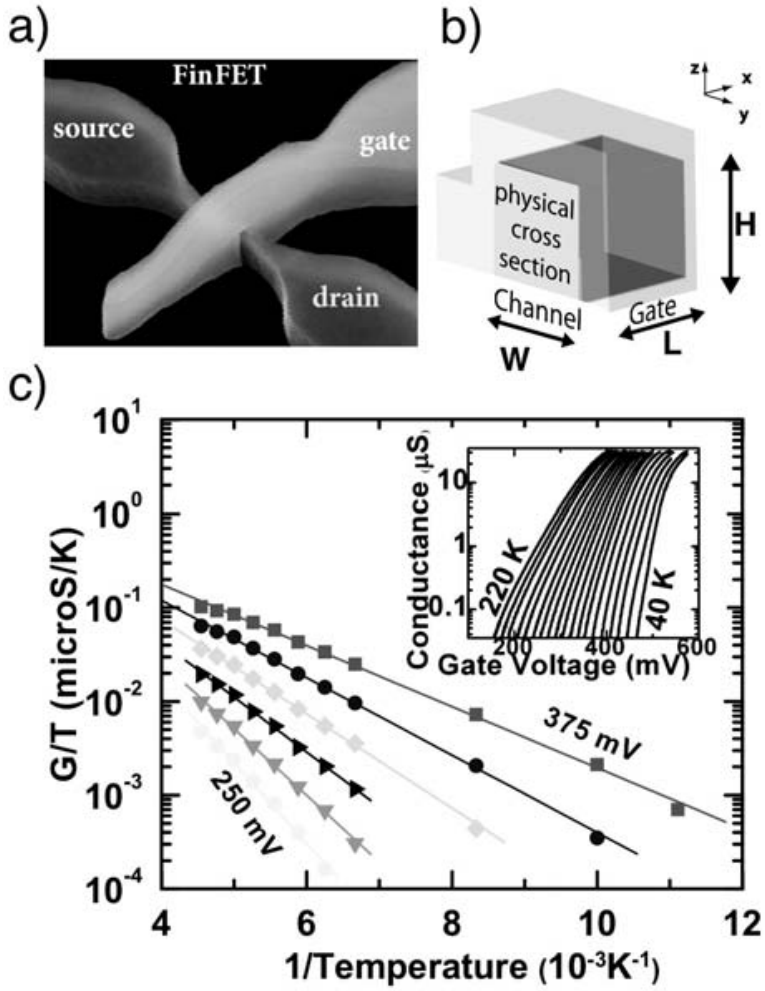

Figure 10.5. (a) Scanning electron microscope (SEM) image of typical FinFETs studied in this section. (b) Schematic view of the FinFETs as in Fig. 10.1 The gate (light yellow) covers three faces of the channel (dark grey). L, H and W represent the channel length, height and width respectively. The physical cross sectional area is shown in light grey. (c) Fits used to extrapolate E_b and S_{AA} in one of our $W = 55$ nm device. In the inset, differential conductance versus V_G data, for different temperatures, are shown.

($W = 25$, 55, 125, and 875 nm) are studied in this section. The discussion focuses on one device for each width since the same behavior for each of the devices of the same width is found consistently. The devices consist of a nanowire channel etched on a 65 nm Si intrinsic film with a wrap-around gate covering three faces of the channel (Fig. 10.5a,b) (Collaert *et al.*, 2005). They have a geometry identical to the ones discussed in Section 10.2 (Sellier

et al., 2007), but their channels are completely undoped. In the devices of this study, an HfSiO layer isolates a TiN layer from the intrinsic Si channel (Collaert *et al.*, 2005). Differential conductance data are taken at $V_{SD} = 0$ mV using a lock-in technique. Fig. 10.5c shows the G / T versus $1000/T$ data obtained from the G versus V_G data taken at different temperatures (inset in Fig. 10.5c).

Using the data of Fig. 10.5c, results for the source (drain)-channel barrier height, E_b, versus V_G dependence and for the active cross-section area of the channel, S_{AA}, versus V_G dependence can be extrapolated using the thermionic fitting procedure as described in Section 10.2. The important fact is that S_{AA} can, also in the undoped case, be interpreted as a good estimation of the portion of the physical cross-section area through which the transport preferentially occurs. Note that Eq. (10.1) has only two parameters, S_{AA} and E_b, and the accuracy obtained in the fits made using this equation[1] demonstrates the validity of the use of this model for the study of sub-threshold transport also in these undoped channel FinFETs.

10.3.3 *Evolution of the Barrier Height with Gate Voltage*

Figure 10.6a examines the barrier height as a function of V_G. An expected decrease in E_b while increasing V_G is observed (as for doped devices, see Fig. 10.2c). The inset of Fig. 10.6a shows that, this effect is less pronounced for a wider device. The decrease is to be attributed to short-channel effects (SCEs) that influence the electronic characteristics even at low bias. This trend is also reflected by the data of Table 10.1, where the coupling factors obtained from our thermionic fits, $\alpha_1 = dE_b/dV_G$,[2] show a decrease for increasing width.

10.3.3.1 Capacitive coupling

In Table 10.1, the coupling between the potential of the channel interface and V_G, α_2, extracted from Coulomb blockade (CB)

[1] $R \sim 0.99$ for all fits of devices with width $\leqslant 125$ nm, as shown in Fig. 10.5c.

[2] See also Section 10.2, thus the electrostatic coupling between the gate and the bulk of the channel.

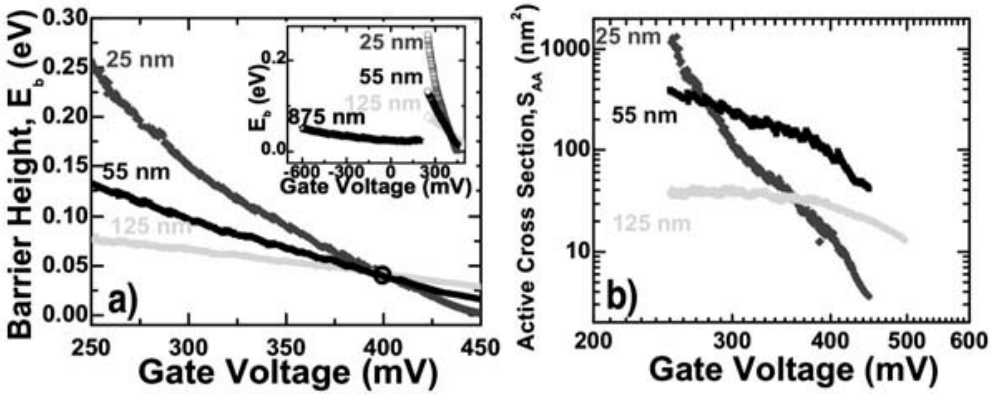

Figure 10.6. Data obtained using the model of Eq. 10.1: (a) E_b versus V_G for one device for each width from 25 nm to 125 nm. In the inset, calculated E_b versus V_G for all device widths are shown. (b) Results of the dependence of the active cross section, S_{AA}, versus V_G obtained for all devices with $W \leqslant$ 125 nm.

Table 10.1. Summary of the characteristics gate channel capacitive coupling of devices reported in this study, obtained from the results of Fit as in Fig. 10.2a (α_1) and from Coulomb Blockage (CB) measurements at 4.2 K (α_2)

Width (nm)	α_1	α_2
25	1	0.7
55	0.7	0.8
125	0.14	0.8
875	0.03	0.8

measurements (at 4.2 K) of confined states that are present at the Channel/Gate interface (Hinds *et al.*, 2000) is also shown. α_2, is found to be a constant independent of W. In CB theory, α_2 is the ratio between the electrochemical potential of the confined states and the change in V_G. This ratio can be estimated from the so-called stability diagram (Sellier *et al.*, 2007) as it is shown in Section 10.2. Overall, these results lead to the conclusion that the coupling to the channel interface remains constant for increasing W, whereas the coupling to the centre of the channel does not. In the 875 nm devices, SCEs are so strong (see inset Fig. 10.6a), that the thermionic theory loses accuracy; hence the results of these devices will not

be discussed any further. All the E_b versus V_G curves, as depicted in Figure 10.6a, cross each other at around 0.4 V (outlined by the black circle), before complete inversion of the channel takes place at $V_{th} \sim 0.5$ V (Collaert *et al.*, 2005). This suggests that for these devices and at $V_G = 0.4$ V, the work function of the TiN is equal to the affinity of the Si channel in our devices (flat bands condition). The same value has also been verified in other measurements using capacitance-voltage ($C-V$) techniques (Singanamalla *et al.*, 2006), independently from the W of the channel. This fact confirm, that, also for these devices, similarly to the ones described in section 10.2, activated transport over the channel barrier is indeed observed. However, for these undoped devices, the barrier is formed by the Metal/Oxide/Semiconductor interface, which at $V_G = 0.4$ V will not dependent on W. The crossing point in Fig. 10.6 (a) is not located exactly at $E_b = 0$ meV, but is at 50 meV. This feature is attributed to the presence, at the Channel-Gate boundary, of interface states (already found in CB measurements) that can store charge, repel electrons and therefore raise-up the barrier by a small amount. In Si/SiO_2 systems that have been studied in the past, these states were estimated to give an energy shift quantifiable between 70 and 120 meV (Hinds *et al.*, 2000), in line with the data of this section.

10.3.4 *Evolution of the Active Cross Section with Gate Voltage*

The data of S_{AA} for these undoped FinFETs show a surprising different evolution with increasing V_G's if compared to what has been observed in the previous section 10.2 for doped channel devices. Fig. 10.6b shows S_{AA} as a function of V_G extrapolated using Eq. (10.1). These results are then compared to the analytical model (Taur, 2000) discussed before and to the self-consistent simulations performed as described in (Neophytou *et al.*, 2008; Paul *et al.*, 2009; Lee *et al.*, 2009; Klimeck *et al.*, 2009). At low V_G, devices with $W = 25$ nm show an active cross sectional area of around 1000 nm^2 (see Fig. 10.6b). This is almost equal to the physical cross sectional area of the channel at these widths. At higher V_G, the active cross sectional decreases to a few nm^2. The interpretation of this data is as follows: at low V_G, transport in these devices is uniformly

distributed everywhere in the physical cross section of the channel (weak volume inversion). But with the increase of V_G, an increase of carrier density in the region near the interface, which leads to a reduction of S_{AA}, arises. This interpretation corresponds with the screening mechanism discussed in Taur (2000). Subsequently the action of the gate on the centre of the channel is suppressed. Devices that have 55 nm and 125 nm widths behave in a fashion similar to the ones with 25 nm, but show a less pronounced decreasing trend and counter intuitive small values for S_{AA}, as a progressive reduction of α_1 (i.e., of the gate-to-channel coupling) for increasing W is indeed observed. This is not a surprise as the barrier in these larger devices is lower and more carriers are allowed to migrate to the interface enhancing the screening effect. These results give, for the first time, an experimental insight into the mechanisms of conduction in undoped FinFETs.

10.3.5 *Comparison with Simulation*

State-of-the-art-simulations, done using an atomistic 10 band $sp^3d^5s^*$ Tight-binding (TB) model (Klimeck *et al.*, 2002; Lee *et al.*, 2009), have been used to perform electronic structure calculation, coupled self-consistently with a 2D Poisson solver (Neophytou *et al.*, 2008), and terminal characteristics using a ballistic top of the barrier (ToB) model (Paul *et al.*, 2009) have been obtained. Due to the extensively large cross-section of the device that combines up to 44,192 atoms in the simulation domain, a new NEMO 3D code (Lee *et al.*, 2009) has been integrated into the top of the barrier analysis (Paul *et al.*, 2009). This expanded modeling capability has made possible to compare experiment and simulations results. The effects of the variation of the potential in the source-drain direction are not expected to play a role in the simulated devices since V_{SD} is very small (Paul *et al.*, 2009; Tettamanzi *et al.*, 2010). Also, the gate length is long enough to suppress the tunneling current from source to drain (Paul *et al.*, 2009; Tettamanzi *et al.*, 2010). In fact, using a geometry identical to the one of the FinFETs used in the experiments discussed in this section, with $W = 25$ nm, $H = 65$ nm and under similar biases, the simulated current distribution shows a crossover from a situation of weak volume inversion at $V_G = 0$ mV (Fig. 10.7a)

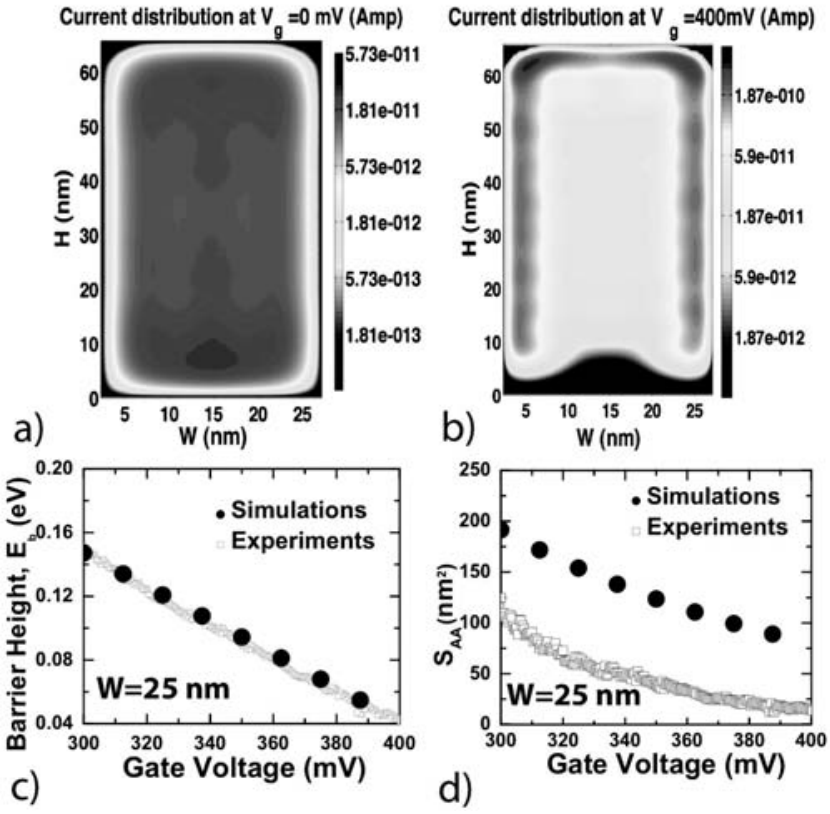

Figure 10.7. Current distributions, for (a) $V_G = 0$ mV, (b) $V_G = 400$ mV, obtained using TB simulations for a geometry having $L = 65$ nm and $W = 25$ nm. Comparison of the simulated (c) E_b and (d) S_{AA} with the experimental data for a $W = 25$ nm device.

to a situation of transport confined prevalently at the interface at $V_G = 400$ mV (Fig. 10.7b).

The simulated spatial current distribution (Fig. 10.7) gives a good indication of where the mobile charges predominately flow in the channel. From calculation too, a reduction of S_{AA} with increasing V_G is obtained (see Fig. 10.7d). However, this reduction is not as sharp as in the experimental data, as these simulations have been performed at $T = 300$ K and also due to the absence of interface states (expected to enhance the effect of screening in real devices as it will be discussed in section 10.4) (Hinds *et al.*, 2000; Sellier *et al.*, 2007). As a final benchmark to this experimental method, the results of the TB simulations have been used to calculate the current and the conductance at different temperatures and to extract, using again Eq. (10.1), simulated E_b and S_{AA} for a $W = 25$ nm device. In fact, in Fig. 10.7c,d, the simulated values are compared to the experiments

and it is found that it is possible to predict experimental results with good accuracy, although the simulations overestimate the values of S_{AA} (probably for the same reasons discussed for Fig. 10.7b). In any case, the comparison between experimental and simulation give a demonstration of the reliability of the method developed in this section (Tettamanzi *et al.*, 2010). This opens the way of its systematic use to obtain information about the magnitude and the position of carriers in FET devices in general and not only in FinFET structures. In these investigations, possible modifications of A^* due to the constrained geometry (Ragi and Romero, 2006) of the devices have been neglected, as it is found to be negligible, and tunneling regimes of transport (Appenzeller *et al.*, 2004) have been excluded due to different temperatures dependences.

10.3.6 *Conclusion*

In conclusion, the results presented in section 10.3 are the first experimental study of the behavior of the active cross-section area as a function of V_G for undoped FinFETs. In particular, conductance traces for a set of undoped FinFETs having the same channel length and height but different width, together with TB simulations for the device of $W = 25$ nm have been presented. For all these small devices ($W \leqslant 125$ nm), a mechanism of inversion of the bands from flat band to band bending in the interface regions respectively, all as a function of V_G, has been proposed and demonstrated. Therefore this section discusses the first-ever direct observation of the theoretical results suggested by Taur. The validity of thermionic approach as a tool for the investigation of sub-threshold transport in undoped FET devices has been confirmed and some answers to the fundamental technological questions, such as how to localize and quantify areas of transport have been provided.

10.4 Interface Trap Density Metrology of Undoped N-FinFETs

10.4.1 *Introduction*

In sections 10.2 and 10.3, it has been demonstrated that, by using thermionic emission, it is possible to measure (1) the active channel

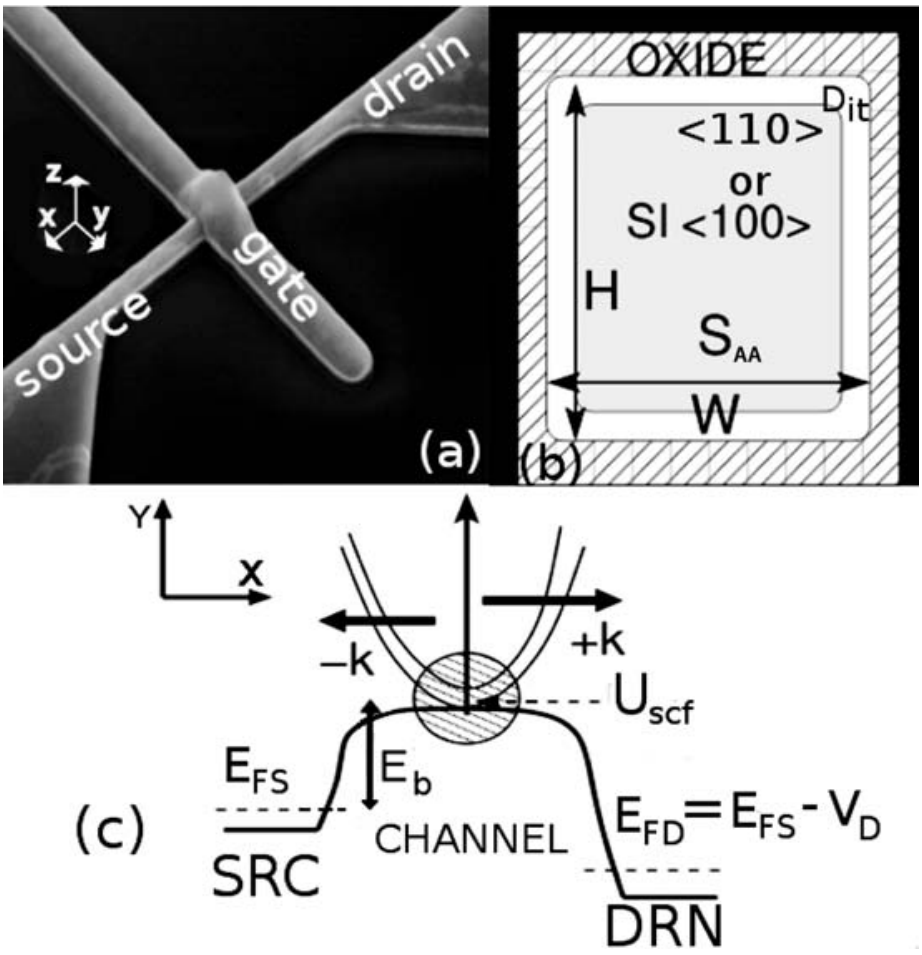

Figure 10.8. (a) Scanning-electron-microscope (SEM) image of a Si n-FinFET with [100] channel orientation and single fin. (b) The schematic of the cross sectional cut in the Y-Z plane of a typical tri-gated FinFET. The active cross-section (S_{AA}) is in gray, H and W are the physical height and width, respectively. (c) Ballistic top of the barrier model employed for calculating the thermionic current in the FinFETs.

cross-section area (S_{AA}) (see Fig. 10.8b), and (2) the source to channel barrier height (E_b), hence opening new ways to investigate FinFETs. Furthermore, in Section 10.3, it was found that for undoped FinFETs, although the trends of the S_{AA} values obtained by mean of experiments and of theoretical simulations were identical, differences in the absolute values were observed. These differences were found to be caused by the presence of interface states at the metal–oxide–semiconductor interface of the experimental devices (Tettamanzi *et al.*, 2010; Lee *et al.*, 2003). These states can trap

electrons and enhance screening, therefore reducing the action of the gate on the channel, and as a final result, a decrease in the absolute value of S_{AA} in the experimental data is observed. Typical D_{it} frequency or time dependent measurements cannot be performed on ultimate devices but only on custom designed structures (Kapila *et al.*, 2007). Such custom structures may only be partially reflective towards the possibly surface orientation-dependent and geometry-dependent D_{it}.

10.4.2 *Aim*

In this section, a simple set of methods for the direct estimation of D_{it} in ultimate devices is provided. The comparison between the values of D_{it} obtained with these two methods and the values obtained using a method implemented in the past (Kapila *et al.*, 2007) show similar trends. A new approach to trap density metrology is of critical importance as CMOS scaling takes device dimensions into the nanometer regime. At these scales, quantities such as D_{it} can vary rapidly with device geometry, rendering old techniques inadequate as they cannot be applied directly in these ultra-scaled devices.

In this section it is shown that by using simple mathematical manipulations and the difference between experimental and simulated values of S_{AA} and of the capacitive coupling, α (see also previous sections), it is possible to infer the value of the interface trap density (D_{it}). Furthermore, to shed more light into the complicated transport phenomena that can arise in these undoped FinFETs, the work of previous sections is expanded and more careful investigations of the evolution of S_{AA} and of E_b are performed. For theoretically investigating these devices, the atomic representation is used. The band structure is obtained using a 10 band $sp^3d^5s^*$ TB model with spin orbit coupling (SO) (Klimeck *et al.*, 2002; Boykin *et al.*, 2004; Neophytou *et al.*, 2008), which is confirmed to be well suited for modeling the band-structure of these confined silicon channels, since TB can easily take into account the material, geometrical, strain and potential fluctuations at the atomic scale (Neophytou *et al.*, 2008). This model takes also into account the coupling of the conduction and the valence bands which is neglected in simple models like the effective

mass approximation (EMA). As shown in Section 10.3, semi-classical "Top of the barrier" (ToB) model accurately captures the thermionic transport (Fig. 10.8c) (Neophytou *et al.*, 2008; Paul *et al.*, 2009; Tettamanzi *et al.*, 2010), the same model can also shed more light on the inner details of the transport, which is discussed next.

10.4.3 *New Implementation of Interface Trap Metrology*

In the undoped devices studied here, qualitatively similar theoretical and experimental trends for the active cross section area versus V_G and barrier height versus V_G are found (Tettamanzi *et al.*, 2010). However, the theoretically obtained values quantitatively over-estimated the experimental values. The reduced experimental values can be attributed to the presence of interface traps in these FinFETs (Tettamanzi *et al.*, 2011; Lee *et al.*, 2003; Kapila *et al.*, 2007). The effect of interface traps on the channel property are even more dominant in the extremely thin FinFETs (Tettamanzi *et al.*, 2011). In this section it is shown how this difference in S_{AA} and E_b can be utilized for the direct estimation of the interface trap density (D_{it}) in FinFETs, thereby eliminating the need to implement special FinFETs geometries to determine D_{it} (Kapila *et al.*, 2007) and providing a new tool for performing interface trap metrology.

This paragraph has been divided into the following sections. Section 10.4.4 provides the details about the FinFETs for which interface trap density metrology has been implemented and the fundamentals of the experimental procedures that are in line with Sections 10.2 and 10.3. The details about the self-consistent calculations are provided in Section 10.4.5 and more insight on the theoretical extraction of E_b and S_{AA} is outlined in Section 10.4.6. Section 10.4.7 provides the details of the two procedures for obtaining the interface trap density. The theoretical and experimental results and the discussion on them are given in Section 10.4.8, while Section 10.4.9 discussed current distributions. The conclusions are summarized in Section 10.4.10.

10.4.4 *Device and Experimental Details*

The undoped n-FinFETs used in this work (A–G, see Table 10.2) consist of nanowire channels etched on a Si intrinsic film with a

Table 10.2. Si n-FinFETs used in the trap metrology study along with their labels. The surface hydrogen annealing detail is also shown. The channel is intrinsic Si, while the source and the drain are n-type doped for all the FinFETs

Label	H (nm)	W (nm)	L (nm)	Channel orientation (X)	H_2 anneal
A	65	25	40	[100]	Yes
B	65	25	40	[100]	No
C	65	~5	40	[100]	No
D	40	18	40	[110]	Yes
E	40	18	40	[110]	Yes
F	40	~3–5	40	[110]	Yes
G	65	~7	40	[100]	Yes

wrap-around gate covering the three faces of the channels (Fig. 10.8a) (Collaert *et al.*, 2005) identical to the ones discussed in Section 10.3. FinFETs with two different channel orientations of [100] ((FinFETs A–C and G)) and [110] ((FinFETs D–F)) have been used (see Table 10.2). All the FinFETs have the same channel length ($L = 40$ nm). The channel height (H) is either 40 nm or 65 nm (Table 10.2). The channel width (W) varies between 3 and 25 nm. An HfSiO (high-κ) layer isolates a TiN layer from the intrinsic Si channel (Collaert *et al.*, 2005). These FinFETs have either one channel (FinFETs A-C and G) or ten channels (FinFETs D-F). These devices have two different surface treatments (with or without H_2 annealing) as shown in Table 10.2.

Measurement procedure: The experimental value of E_b and S_{AA} are obtained using the differential conductance method introduced in sections 10.2 and 10.3. The conductance data are taken at $V_{SD} = 0$ V using a lock-in technique. The full experimental method and the required ambient conditions have been outlined in detail in (Tettamanzi *et al.*, 2010). In the next section we discuss the theoretical approach to calculate the values of E_b and S_{AA} in tri-gated n-FinFETs.

10.4.5 *Modeling Approach*

To obtain the self-consistent charge and potential and transport characteristics in the n-FinFETs, the electronic structure is

calculated using an atomistic 10 band $sp^3d^5s^*$ semi-empirical TB (Klimeck *et al.*, 2002) as discussed in Section 10.3. Using thermionic fitting procedure (Tettamanzi *et al.*, 2010), E_b, α and S_{AA} can be extracted using the experimental and theoretical conductance (G) using Eq. (10.1) for a 3D system (Sze, 1981). This equation will hold only when the cross-section size of the FinFET is large enough (i.e., W, $H > 20$ nm) to be considered a 3D bulk system. In this study, S_{AA} is extracted for FinFETs with W(H) $\approx$ 25 nm (65 nm). When the $3D$ approximation is not true anymore (i.e., W or $H \lesssim 20$ nm), only E_b and α can be correctly extrapolated (Tettamanzi *et al.*, 2010). Since the FinFETs studied here show (i) negligible source-to-drain tunneling current and (ii) reduced SCEs (Tettamanzi *et al.*, 2010), the ToB model is applicable to such devices (Paul *et al.*, 2009). For the simulations, all the FinFETs are n-type doped in the source and drain to a value of 5×10^{19} cm^{-3}. A 1.5 nm SiO_2 cover is assumed. Next the procedure used to calculate E_b and S_{AA} are discussed more in detail.

10.4.6 *Extraction of Barrier Height and the Active Cross Area Section*

For pure thermionic emission any carrier energetic enough to surmount the barrier from the source to the channel (C) (Fig. 10.8c) will reach the drain provided the transport in the channel is close to ballistic. The source/drain in FETs are typically close to thermal and electrical equilibrium (since heavy scattering in the contacts is assumed which leads to instantaneous carrier relaxation). This allows the use of the realistic assumption that most of the carriers in the Source/Drain are thermalized at their respective Fermi-levels (E_{fs}, E_{fd} in Fig. 10.8c). Also the channel potential (U_{scf}) can be determined under the application of V_G using the self-consistent scheme (Paul *et al.*, 2009; Lee *et al.*, 2009). Hence, for the source-to-channel homo-junction inside a FET, the barrier height (E_b) can be determined as a function of V_G,

$$E_b(V_G) = U_{scf}(V_G) - E_{fs}. \tag{10.2}$$

This definition of E_b implicitly contains the temperature dependence since the simulations are performed at different temperatures

(T) which feature in the Fermi distribution of the Source/Drain, but, as it will be shown in Section 10.4.8, the temperature dependence of E_b in the sub-threshold region is very weak. Therefore, all the theoretical E_b results shown in this chapter are at $T \approx 300$ K.

The study of thermionic emission model is applicable when the barrier height is much larger than the thermal broadening ($E_b \gg k_B T$ (Sze, 1981)). For this reason, Eq. (10.2) works only in the sub-threshold region where E_b is well defined (Paul *et al.*, 2009) and once the FinFET is above the threshold, E_b ($\leq K_B T$) is not a well-defined quantity anymore (Paul *et al.*, 2009). Furthermore, when the cross-section size of the FinFET is not large enough (i.e., W, $H \leqslant 20$ nm) to be considered in a 3D bulk limit, S_{AA} cannot be extracted using Eq. (10.1) since the system is close to 1D. For a 1D system the G, under a small drain bias (V_{SD}) at a temperature T, is given by the following (for a single energy band),

$$G_{1D} = \frac{2e^2}{h} \cdot \left[1 + exp\left(\frac{E_b(V_G)}{k_B T}\right)\right]^{-1} \tag{10.3}$$

where h is the Planck's constant. Since Eq. (10.3) lacks any area description, G for 1D systems is no more a good method to extract S_{AA}. Below we will present an approach to solve this problem and to distinguish a 1D system from a 3D system. A part of all these limitations and as described in Sections 10.2 and 10.3, S_{AA} can be extracted using Eq. (10.1).

10.4.7 *Trap Extraction Methods*

In Tettamanzi *et al.* (2010) (see also Section 10.3), it was observed that the active cross-section area ($S_{AA,sim}$) obtained theoretically is over-estimating the experimental value ($S_{AA,exp}$). In Section 10.4.8 it will be further shown that also the theoretical E_b value can over estimate the experimental E_b value. These mismatches can be attributed to the presence of traps at the oxide–channel interface of multi-gate FETs where these traps can enhance the electro-static screening and suppress the action of the gate on the channel (Kapila *et al.*, 2007; Lee *et al.*, 2003; Tettamanzi *et al.*, 2010). This simple idea is a powerful tool used for the estimation of interface trap density (D_{it}) in these undoped Si n-FinFETs.

10.4.7.1 Method I: D_{it} from active area

Based on the difference between the simulated and the experimental active area (S_{AA}) values, a method to calculate the density of interface trap charges, σ_{it}, in the FinFETs is outlined. The method is based on the assumption that the total charge in the channel at a given V_G must be the same in the experiments and in the simulations. This requirement leads to the following:

$$S_{AA,sim} \cdot L_{ch} \cdot \rho_{sim} = S_{AA,expt} \cdot L_{ch} \cdot \rho_{expt} + e \cdot \sigma_{it} \cdot L_{ch} \cdot P \quad (10.4)$$

where $S_{AA,sim}$ ($S_{AA,expt}$) is the simulated (experimental) active area, P is the perimeter of the channel under the gate ($P = W + 2H$) and ρ_{sim} (ρ_{expt}) is the simulated (experimental) charge density. Close to the oxide channel interface it is possible to locally assume that ρ_{expt} is obtained from ρ_{sim} and σ_{it} as,

$$\rho_{expt} = \rho_{sim} - \rho_{it} = \rho_{sim} - (e \cdot \sigma_{it} \cdot P)/(W \cdot H) \quad (10.5)$$

Using Eqs. (10.4) and (10.5) the final expression for σ_{it} is obtained as,

$$\sigma_{it}(V_G) = \frac{\rho_{sim}(V_G) S_{AA,sim}(V_G)}{e \cdot P} \times \left[\frac{\left[1 - \frac{S_{AA,expt}(V_G)}{S_{AA,sim}(V_G)}\right]}{\left[1 - \frac{S_{AA,expt}(V_{gs})}{W \cdot H}\right]} \right] \quad [\#/\mathrm{cm}^2] \quad (10.6)$$

This method is useful for wider devices for which Eq. (10.1) is valid. For very thin FinFETs (close to a 1D system) this method cannot be utilized.

Assumptions in Method I: In the calculation of σ_{it} several assumptions were made. The extra charge contribution completely stems from the interface trap density (D_{it}) and any contribution from the bulk trap states has been neglected. Also all the interface traps are assumed to be completely filled which implies $\sigma_{it} \cong D_{it}$. This method of extraction works best for undoped channel since any filling of the impurity/dopant states is neglected in the calculation. Also the interface trap density is assumed to constant for the top and the side walls of the FinFET which is generally not the case (Kapila *et al.*, 2007; Lee *et al.*, 2003). Orientation-dependent D_{it} for different surfaces could be included as a further refinement.

10.4.7.2 Method II: D_{it} from barrier control

The second method does not utilize the E_b value directly but its derivative w.r.t. V_G. The term $\alpha = |dE_b/dV_G|$ represents the channel to gate coupling (Sellier *et al.*, 2007; Tettamanzi *et al.*, 2010). The presence of interface traps weakens this coupling due to the electrostatic screening. This method of trap extraction is based on the difference in the experimental and the simulated α value. The α value can be represented in terms of the channel and the oxide capacitance. The equivalent capacitance model for a MOSFET with and without interface traps (D_{it}) is shown in Fig. 10.9. The α value can be associated with the oxide, interface, and semiconductor capacitance, which is given in Eq. (38) on page 383 in Sze (1981). This relation leads to the following:

$$\left|\frac{dE_b}{dV_G}\right| = 1 - \frac{C_{tot}}{C_{ox}}, \tag{10.7}$$

where C_{tot} is the total capacitance. For the two cases, as shown in Fig. 10.9, the total capacitance is given by

$$C_{tot}^{exp} = \frac{C_{ox} \cdot (C_d + C_{it})}{C_d + C_{ox} + C_{it}}, \tag{10.8}$$

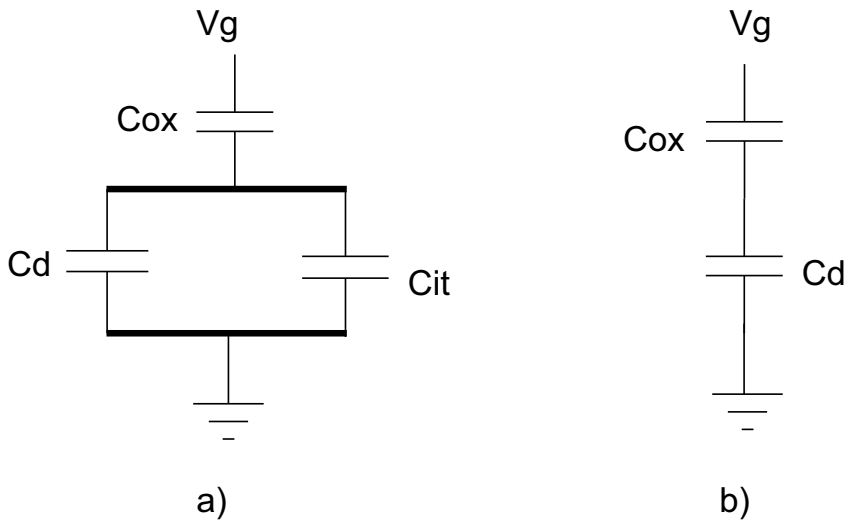

Figure 10.9. Equivalent circuits (a) with interface-trap capacitance (C_{it}) and (b) without interface capacitance. C_d and C_{ox} are the depletion and the oxide capacitance, respectively. The idea for this equivalent circuit is obtained from page 381 in Sze (1981).

$$C_{tot}^{sim} = \frac{C_d \cdot C_{ox}}{C_d + C_{ox}}, \tag{10.9}$$

where C_{it}, C_{ox}, and C_d are the interface trap capacitance, the oxide capacitance and the semi-conductor capacitance, respectively. Eq. (10.8) represents the capacitance in the experimental device and Eq. (10.9) represents the capacitance in the simulated device under ideal conditions without any interface traps. Combining Eqs. (10.7), (10.8), and (10.9) and after some mathematical manipulations, it is possible to obtain,

$$\frac{1}{\alpha_{exp}} = \frac{1}{\alpha_{sim}} + \frac{C_{it}}{C_{ox}}, \tag{10.10}$$

Manipulating Eq. (10.10) gives the following relation for C_{it}

$$C_{it} = C_{ox} \cdot \left(\frac{1}{\alpha_{sim}}\right) \cdot \left[\frac{\alpha_{sim}}{\alpha_{exp}} - 1\right] \tag{10.11}$$

Also C_{it} can be related to the interface charge density (σ_{it}) as (Sze, 1981),

$$C_{it} = e \cdot \frac{\partial \sigma_{it}}{\partial V_G} \tag{10.12}$$

where e is the electronic charge. In Eq. (10.11) all the values are dependent on V_G except C_{ox}. Combining Eqs. 10.11 and 10.12 and integrating w.r.t. V_G yields the final expression for the integrated interface charge density in these FinFETs as

$$\sigma_{it} = \frac{C_{ox}}{e} \cdot \int_{V1}^{V2=V_{th}} \left(\frac{1}{\alpha_{sim}(V_G)}\right) \times \left[\frac{\alpha_{sim}(V_G)}{\alpha_{exp}(V_G)} - 1\right] dV_G \quad [\#/\mathrm{cm}^2], \tag{10.13}$$

where V_{th} is the threshold voltage of the FinFET and V1 is the minimum V_G for which $\alpha_{exp/sim}$ is $\approx$ 1. Of course, the integration range for Eq. (10.13) is in the sub-threshold region. This method has the advantage that it is independent of the dimensionality of the FinFET. Hence, Eq. (10.13) can be used for wide as well as for thin FinFETs.

Assumptions in Method II: The most important assumption is that the rate of change of the surface potential ($\Psi(V_G)$) is the same as E_b w.r.t. V_G. The extra charge contribution completely originates from

the density of interface trap charges (σ_{it}) and any contribution from the bulk trap states have been neglected. Also all the interface traps are assumed to be completely filled which implies $\sigma_{it} = D_{it}$. This method works best when the change in the DC and the AC signal is low enough, such that the interface traps can follow the change in the bias sweep (Sze, 1981).

10.4.7.3 Limitations of the methods

To apply these trap metrology methods properly, is important to understand their limitations, which are presented in this section. One of the main limitation is how closely the simulated FinFET structure resembles the experimental device structure. This depends both on the SEM/TEM imaging as well the type of simulator used. In the present case a FinFET cross-section structure is created by using the TEM image making the simulated structure as close to the experimental device as possible. With the development of better TCAD tools, the proximity of the simulated structure to experimental structure has increased. This allows good confidence in the simulated conductance values then used for the interface trap calculations. Furthermore, the simulated G is calculated as close to ideal as possible and all the differences between the ideal and experimental G are attributed to the traps, which may not be true always. An important difference between the two methods is that they are calculated over different V_G ranges. This is important since the trap filling and their behavior changes within the V_G range which should be taken into account accurately. One must also be aware of the embedded assumption of complete interface trap filling and the neglect of the bulk traps.

10.4.8 *Results and Discussion*

In this section the theoretical results as well as their comparison with the experimental data are provided and discussed.

10.4.8.1 Temperature dependence of the barrier height

The source-to-channel barrier height has been assumed to be temperature independent in the sub-threshold region. Figure 10.10

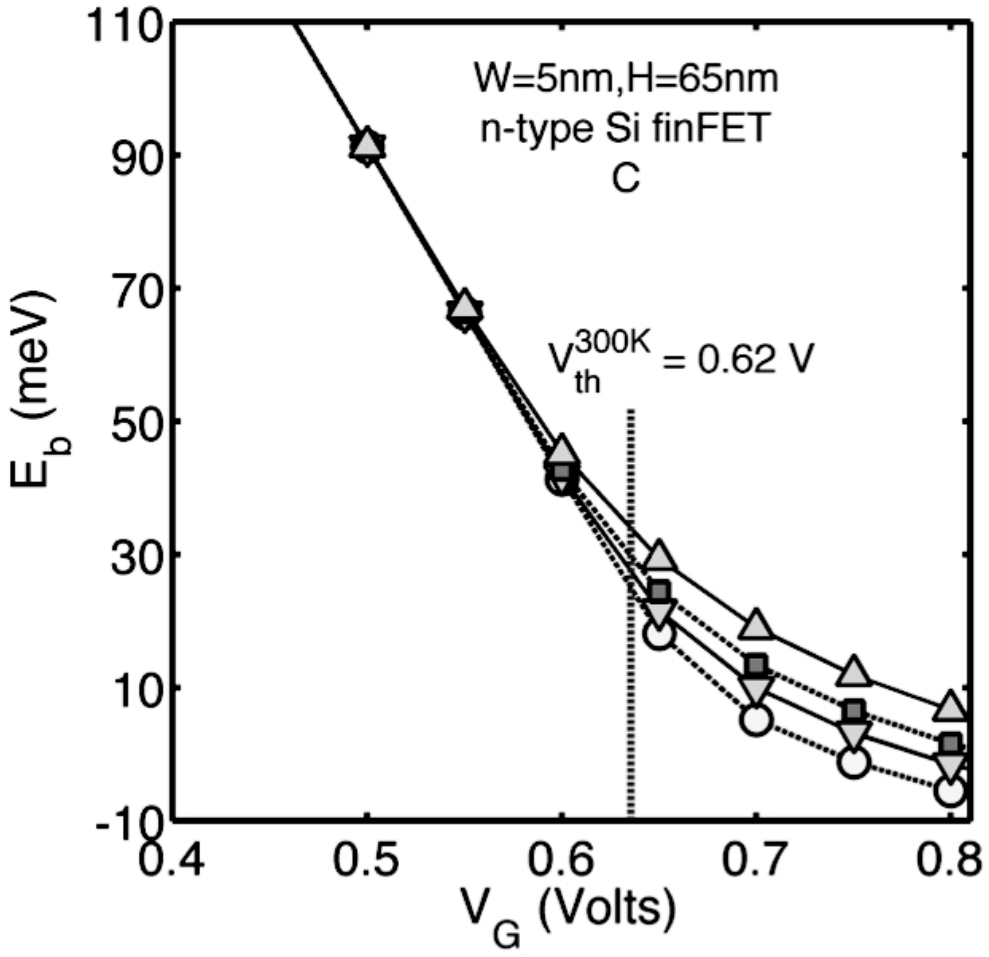

Figure 10.10. Temperature dependence of the simulated barrier height (E_b) in the n-FinFET C from 140 K to 300 K, (circle are for 140 K, down triangles for 200 K, squares for 240 K and up triangles for 300 K). At $T = 300$ K, V_{th} of the FinFET is 0.62 V. The overlap of the curves at different temperatures with V_G, below V_{th} at 300 K, shows a weak temperature dependence of E_b in the sub-threshold region. The impact of temperature becomes prominent after V_G goes above V_{th}.

shows the results of a temperature dependent ToB calculations and proves that the barrier height (E_b) is only weakly temperature dependent in the sub-threshold regime. In the subthreshold region, the E_b value for FinFET C, is same at four different temperatures ($T = 140$ K, 200 K, 240 K and 300 K). The variation with temperature becomes more prominent when the FinFET transitions into the on-state. Since, E_b has a weak temperature dependence in the

sub-threshold region it is then possible to evaluate E_b from the 300 K simulations only.

10.4.8.2 Evolution of the barrier height and of the active cross-section area with V_G

Experimentally, it has been shown that for undoped silicon n-FinFETs (Tettamanzi *et al.*, 2010), E_b reduces as V_G increases. Theoretically, the E_b value is determined using Eq. (10.2), which depends on the self-consistent channel potential (U_{scf}). As the gate bias increases, the channel can support more charge. This is obtained by pushing the channel conduction band lower in energy to be populated more by the source and drain Fermi level (Neophytou *et al.*, 2008). Figures 10.11 and 10.12 show the experimental and theoretical evolution of E_b in FinFETs G, C and D, E, respectively. Theory provides correct quantitative trend for E_b with V_G. *Few important observations here are, (i) theoretical E_b value is always higher than experimental value and (ii) [110] Si devices (D and E) show larger mismatch to the experimental values.* The reason for the first point is suggested to be the presence of interface traps in the FinFETs which screen the gate from the channel (Tettamanzi

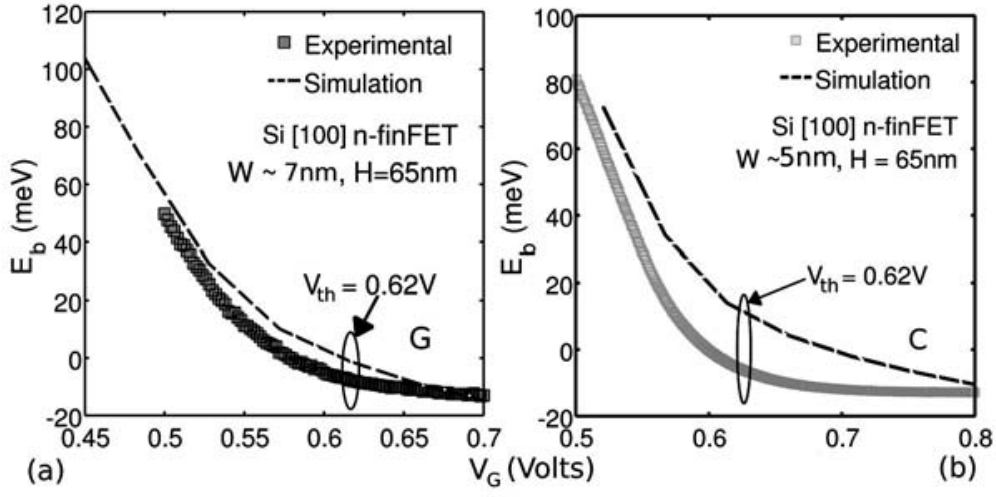

Figure 10.11. Experimental and simulated barrier height (E_b) in n-FinFET (a) G and (b) C. Both the devices have same V_{th}. Both experiment and simulation show a decreasing value of E_b with V_G, but the absolute values are different.

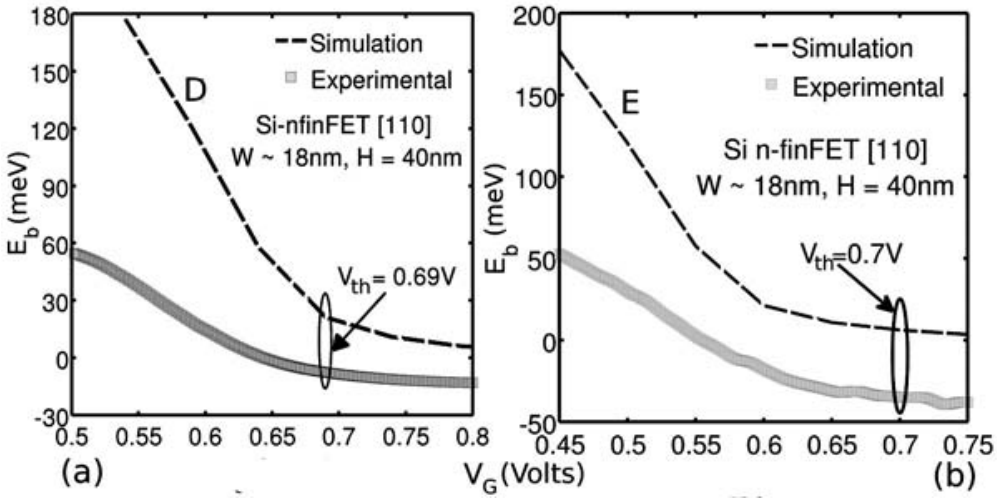

Figure 10.12. Experimental and simulated barrier height (E_b) in n-FinFETs (a) D and (b) E. Both the devices have similar V_{th}. Both experiment and simulation show a decreasing value of E_b with V_G, but the absolute values are different.

et al., 2010). The second observation can be understood by the fact that [110] channels with (110) sidewalls have more interface trap density due to the higher surface bond density (Sze, 1981) and bad etching on the (110) sidewalls (Kapila *et al.*, 2007).

The active cross section area (S_{AA}) represents the part of the channel where the charge flows (Tettamanzi *et al.*, 2010). Experimentally S_{AA} is shown to be decreasing with gate bias since the inversion charge moves closer to the interface that electrostatically screens the inner part of the channel from the gate (Tettamanzi *et al.*, 2010, 2011). This gives a good indication of how much channel area is used for transporting the charge. Figure 10.13a,b show the experimental evolution of S_{AA} in FinFET B and E, respectively. The theoretical value of S_{AA} decreases with V_G which is in qualitative agreement to the experimental observation (Tettamanzi *et al.*, 2010). However, the absolute values do not match. In fact theory over-estimates the experimental S_{AA} value (Fig. 10.13), which is attributed to the interface traps.

10.4.8.3 Trap density evaluation

In this section the results on D_{it} in the undoped Si n-FinFETs are presented:

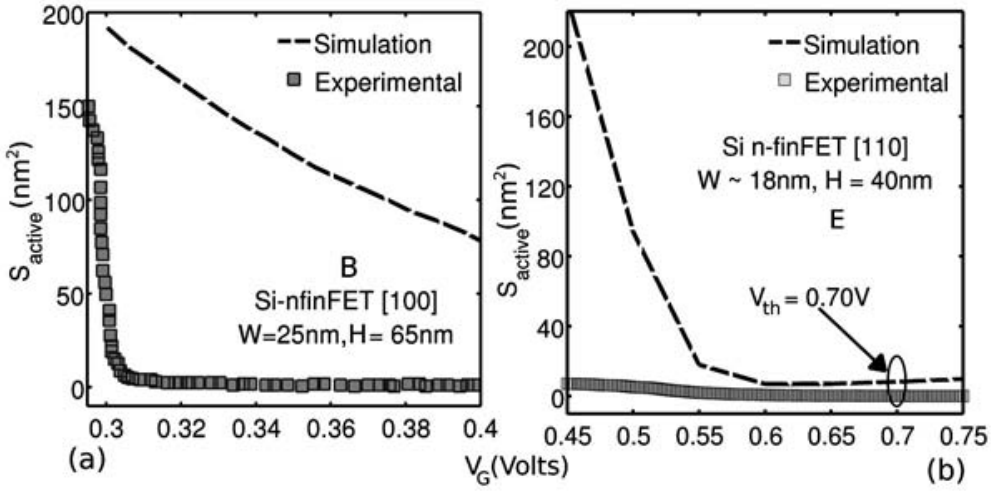

Figure 10.13. Experimental and simulated channel active cross-section (S_{AA}) in n-FinFETs (a) B and (b) E. Both experiment and simulation show a decreasing value of S_{AA} with V_G, but the absolute values are different.

D_{it} using S_{AA}: method I

This approach is based on method I (see section 10.4.7 for details). The calculated D_{it} values for FinFET B and E are 1.06e12 cm^{-2} and 1.81e12 cm^{-2} (Fig. 10.14 (a) and (b), respectively). The D_{it} values compare quite well with the experimental D_{it} values presented in (Kapila *et al.*, 2007) and also shown in Table 10.3. As expected the D_{it} value for FinFET E (with [110] channel and (110) sidewalls) is

Table 10.3. Values of D_{it} obtained from all the n-FinFETs

Device	Method	D_{it} (10^{11} cm^{-2})	FET type	Obs.
$L = 140$ nm*	Charge	1.725	Special body	—
$L = 240$ nm*	Pumping	2.072	tied FET	—
A	I	5.560	Std. FET	H_2 anneal, reduces D_{it}
B	I	10.60	Std. FET	
	II	8.860	Std. FET	
C	II	9.26	Std. FET	Thin fin, more D_{it}
D	II	18.31	Std. FET	(110) side-wall, thin fin, more etching, more D_{it}
E	I	18.1	Std. FET	
	II	15.3	Std. FET	
F	II	36.3	Std. FET	
G	II	4.33	Std. FET	H_2 anneal, less D_{it}

Source: From Kapila *et al.* (2007).

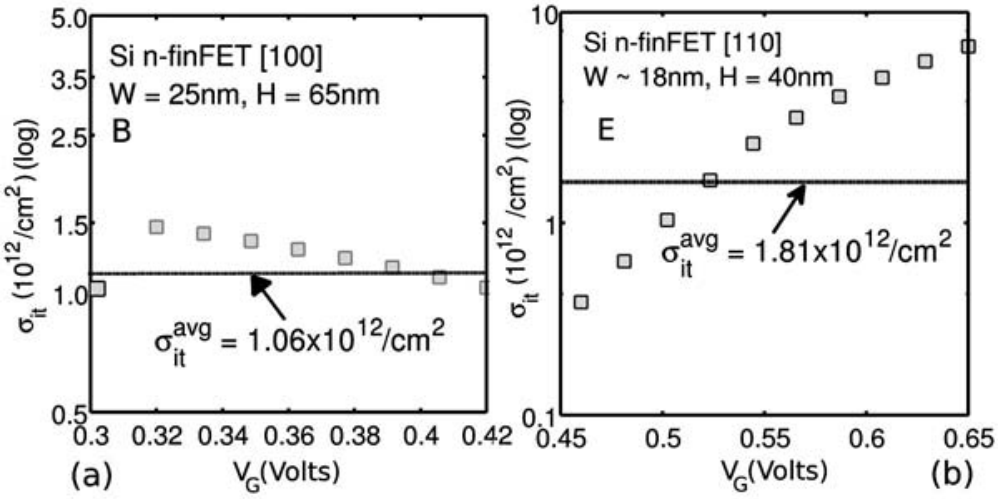

Figure 10.14. Extracted trap density using the difference in active device area (method I) for n-FinFETs (a) B and (b) E.

higher than FinFET B ([100] channel with (100) sidewalls). This is attributed to the higher D_{it} ($\sim 2\times$) on the (110) surfaces (Kapila *et al.*, 2007). The results presented in this section show $\sim 1.8\times$ more D_{it} for (110) sidewalls, in close agreement to previous experiments (Kapila *et al.*, 2007). This method allows to calculate the D_{it} in the actual FinFETs rather than custom made FETs.

D_{it} using $-dE_b/dV_G$ |: Method II

This approach is based on method II (see section 10.4.7 for details). The C_{ox} value, needed in this method, is taken as $\sim$0.0173 F/m^2, which is assumed to be the same for all the devices since these FinFETs have similar oxide thickness. The calculated D_{it} values for FinFET C and E are 9.26e11 cm^{-2} and 1.563e12 cm^{-2} (Fig.10.15 (a) and (b), respectively). These calculations also show that [110] channel device (FinFET E) shows higher D_{it} compared to the [100] channel device (FinFET C), again consistent with the observations made in (Kapila *et al.*, 2007). The advantage of this method is that it can be used to obtain D_{it} in extremely thin FinFETs (close to 1D system) unlike method I which is applicable only to wider FinFETs (due to the reasons discussed in section 10.4.6).

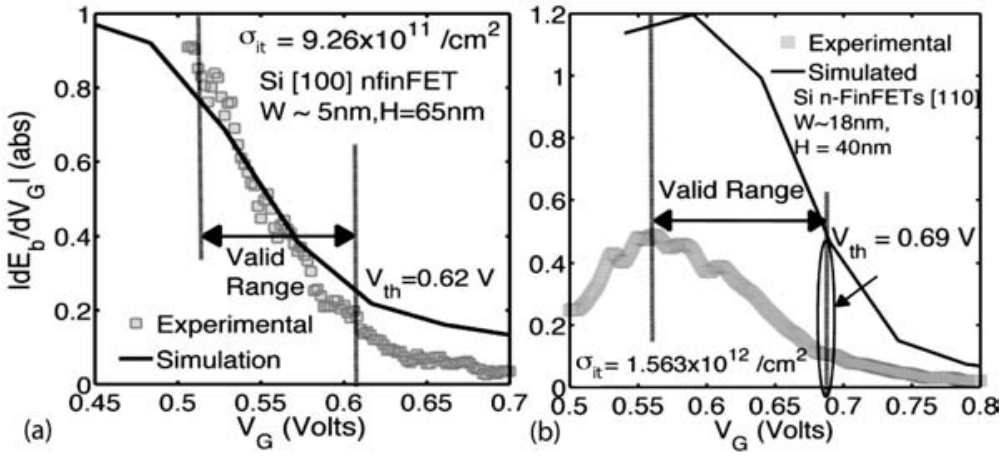

Figure 10.15. Experimental and simulated value of α in n-FinFETs (a) C and (b) E.

10.4.8.4 Discussion of the two methods and D_{it} trends

The D_{it} values for all the FinFETs used in this study are shown in Table 10.3. The important outcomes about the two methods are outlined below:

- The D_{it} values obtained by the two methods compare very well with the experimental measurement in (Kapila *et al.*, 2007) for similar sized FinFETs (A and B). This shows the validity of these new methods.
- The D_{it} values calculated using method I and II (for B and E) compare very well with each other which shows that the two methods are complimentary (Tettamanzi *et al.*, 2011).
- The D_{it} values calculated for the two similar FinFETs (E and F) compare very well showing the reproducibility of the methods.

The calculated D_{it} values also reflect some important trends about the FinFET width scaling and surfaces (Table 10.3). The central points are

- Hydrogen passivation considerably reduces D_{it} (Lee *et al.*, 2003). This is observed for FinFETs A and B where H_2 passivation results in $\sim 2\times$ less D_{it} in FinFET A.

- Width scaling requires more etching which also increases D_{it} (Kapila *et al.*, 2007). The same trend is observed in devices A to C and D to F (decreasing *W*).
- (110) sidewalls show higher D_{it} compared to (100) sidewalls (Kapila *et al.*, 2007). The same trend is also observed for FinFETs A, B, C, G ((100) sidewall) compared to FinFETs D, E, and F ((110) sidewall).

10.4.9 *Current Distribution*

The charge flow in n-FinFETs shows a very strong dependence on the geometrical confinement. For very small width FinFET the entire body gets inverted and shows a very little change in S_{AA} with V_G. For wider FinFETs the current flow starts from a weak volume inversion and moves to surface inversion as V_G increases (Tettamanzi *et al.*, 2010). The theoretical spatial current calculation reveals similar trend which is shown in Fig. 10.16 For extremely thin

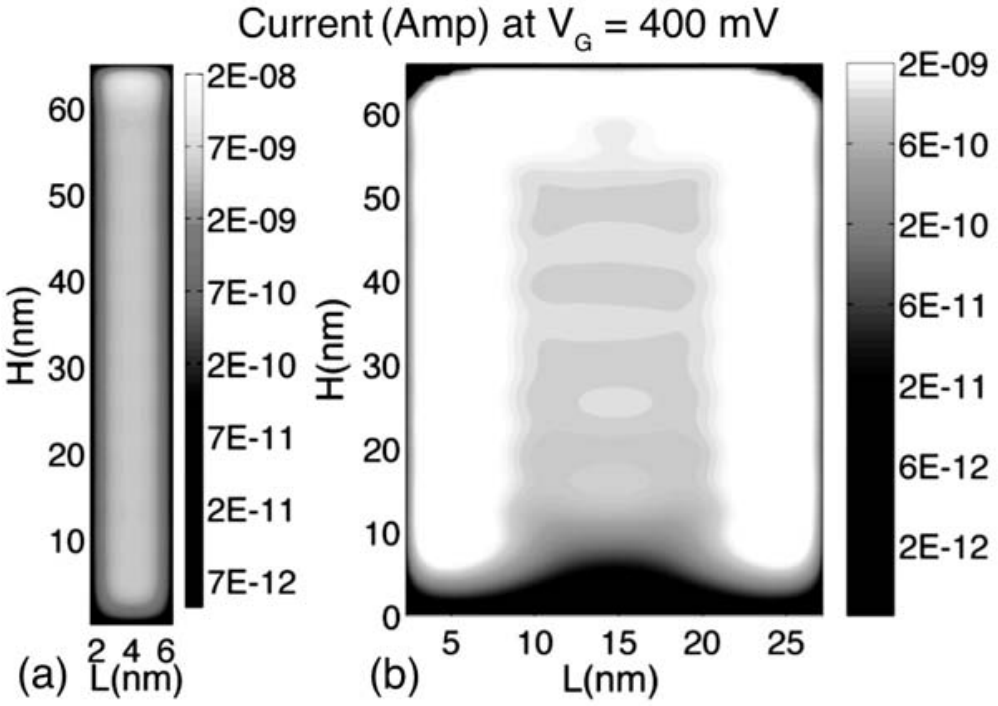

Figure 10.16. Simulated spatial current distribution in the [100] undoped Si n-FinFET intrinsic with H = 65 nm and (a) W = 5 nm and (b) W = 25 nm. V_G = 0.4 V and V_{SD} = 30 mV at 300 K. 5 nm device shows a complete volume inversion. In the 25 nm device the current mainly flows at the edges.

n-FinFETs ($W = 5$ nm, $H = 65$ nm) the charge flow is prevalently through the entire body (volume inversion) compared to the wider n-FinFETs ($W = 25$ nm, $H = 65$ nm) where the charge flows at the edges. This reflects the fact that thinner FinFETs show better channel area utilisation for the charge flow. However, an important practical limitation comes from the fact that extremely thin FinFETs also require more etching, which increases D_{it} and hence can limit the action of thin FinFETs. The advancement of fabrication methods and strain technology may improve the performance of thin FinFETs as shown by some experimental works (Wong, 2002).

10.4.10 *Conclusion*

A new D_{it} determination methodology for state-of-the-art n-FinFETs is presented. Two complementary approaches provide (a) the gate bias (V_G) dependence of D_{it} (Method I) and, (b) the total D_{it} (Method II).

The following trends are observed:

(i) The hydrogen annealing step in the fabrication process substantially reduces D_{it} in good agreement with Ref. (Lee *et al.*, 2003)
(ii) The scaling of the W of the devices (i.e., from A to C or from D (E) to F) increases the density of interface states
(iii) The change in the orientation of the channel (and therefore the sidewall surface where the interface traps are formed) from [100] (device A or C) to [110] (device D (E) or F) remarkably increases the density of interface states
(iv) By comparison of the value of D_{it} obtained for device B in the two approaches (i.e., see Fig. 10.13 and Table 10.3) and the value of D_{it} obtained for two identical devices (D and E) using the same approach (Method II), compatibility and reproducibility of the methods are demonstrated.

The reported trends are similar to the one suggested in the literature (Lee *et al.*, 2003; Xiong *et al.*, 2004). The simple Top-of-the-barrier model, combined with Tight-binding calculations, explains very well the thermally activated sub-threshold transport in state-of-the-art Si FinFETs. The qualitative evolution of E_b and S_{AA} with V_G are

well explained by the theory. Furthermore, the mismatch in the quantitative values of E_b and S_{AA} led to the development of two new interface trap density calculation methods. The advantage of these methods is that they do not require any special structure as needed by the present experimental methods. Hence the interface quality of the ultimate channel can be obtained. These methods are shown to provide consistent and reproducible results which compare very well with the independent experimental trap measurement results. The calculated trends of interface trap density with channel width scaling, channel orientation and hydrogen passivation of the surfaces compare well with the experimental observations. The volume inversion observed in thin width FinFETs is more efficient, in term of volume utilization. However, it could lead to a better utilization of FETs channel only if surfaces roughness and the density of interface traps, created during the extreme etching necessary for these device to be fabricated, can be reduced.

10.5 Final Conclusions

This chapter discusses how, by making use of a classical tool such as the thermionic emission theory in combination with state-of-the-art tight binding simulations, it is possible to provide precious information on the transport characteristics of ultra-scaled Si n-FinFETs. In fact, it is demonstrated here that the amplitude of the energy barrier, of the region of transport in the channel and of the interface trap density, are all quantities that can be directly estimated in state-of-the-art FinFETs. Due to the rapid scaling of CMOS-FET technology, the techniques introduced in this chapter could become routine tools for device improvement and optimization.

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Chapter 11

Dopant Metrology in Advanced FinFETs

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11.1 Introduction

Ultra-scaled FinFET transistors bear unique fingerprint-like device-to-device differences attributed to random single impurities. This chapter describes how, through correlation of experimental data with multimillion atom tight-binding simulations using the NEMO 3-D code, it is possible to identify the impurity's chemical species and determine their concentration, local electric field and depth below the Si/SiO_2 interface. The ability to model the excited states rather than just the ground state is the critical component of

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the analysis and allows the demonstration of a new approach to atomistic impurity metrology.

11.2 Recent Progress in Donor Spectroscopy

Modern transistors are getting so small that it is increasingly difficult to use traditional techniques for their study and their characterisation (Sze, 1981). This is particularly true for the identification of the impurity chemical species present in the channel and for the quantification of their concentration. Different groups have recently investigated the effects of ultra-scaling in silicon field effect transistor (FET) geometries and interesting results have emerged:

- Bjork *et al.* (2008) have shown that screening due to interface traps in ultra-scaled silicon nanowires can cause substantial increase on the ionization energy of the dopant. This result has profound implications for the design of future FET devices.
- Pierre *et al.* (2010) and Wacquez *et al.* (2010) have shown that the presence of a single dopant in the channel of a trigate FET can dramatically alter its electrical signature, even at room temperature.
- Fuechsle *et al.* (2010) have studied the band structure effects on single-crystal silicon geometries for which the source, the drain and the gates are fabricated using an atomically sharp doping procedure (Schofield *et al.*, 2003). Therefore they have investigated on the consequences of scaling a device up to the single atom limit.
- Tabe *et al.* (2010) have demonstrated that, in ultra scaled silicon FET devices, even in the presence of a dopant-rich environment, it is possible to observe the signature of a single dopant.

Overall, all these studies have allowed a better understanding of the effects that arise due to the ultra-scaled environment, however, they have also indicated that, for the successful design of fu-

ture Complementary-Metal-Oxide-Semiconductor (CMOS) devices, a substantial amount of knowledge is still missing. As an example it is not yet clear how CMOS technology will be able to overcome critical challenges such as scaling-induced variability of device characteristics (Wacquez *et al.*, 2010; Asenov, 1999).

As a consequence, it is of interest to discuss in detail a method that can be used to demonstrate atomic impurity metrology (Lansbergen *et al.*, 2008a,b). In fact, through correlation of experimental data with multimillion atom simulations in NEMO 3-D, the impurity's chemical species can be identified and their concentration, local electric field and depth below the Si/SiO_2 interface can be determined (Lansbergen *et al.*, 2008a,b). Furthermore, the extension of the dopants in the source/drain (S/D) regions can be measured by spectroscopy of confined states in the channel (Lansbergen *et al.*, 2008a,b). Lastly, the effective current distribution in the channel can be determined by means of thermionic emission theory (Sellier *et al.*, 2007). Following these lines, the goal of this chapter is to introduce a new dopant metrology technique to be used for ultra-scaled CMOS devices.

11.3 Transport-Based Dopant Metrology in Advanced FinFETS

Direct or impurity-mediated tunnelling between source and drain competes with the thermally activated current and thereby affects the sub-threshold swing. Advanced Si MOSFET devices have shrunk to dimensions where the magnitude of the sub-threshold swing is dominated by the nature of individual impurities in the channel region. Due to the random nature of the impurity distribution, parameters such as excited band levels (Fuechsle *et al.*, 2010), ionization energy, threshold voltage and leakage current show device-to-device fluctuations (Asenov, 1999; Ono *et al.*, 2007; Khalafalla *et al.*, 2007, 2009; Tabe *et al.*, 2010; Pierre *et al.*, 2010; Wacquez *et al.*, 2010; Bjork *et al.*, 2008). An atomistic point of view is imperative to understand and determine the underlying donor characteristics in the channel. Several recent experiments have showed that the fingerprint of a single dopant can be identified

in low-temperature transport through such devices (Calvet *et al.*, 2007; Hofheinz *et al.*, 2006; Tabe *et al.*, 2010; Pierre *et al.*, 2010; Wacquez *et al.*, 2010; Lansbergen *et al.*, 2008b; Sellier *et al.*, 2006), suggesting a new method to characterize devices down to the level of a single impurity. In the context of quantum state control in quantum computing, it was shown that it is possible to model the orbital levels of a single donor in the channel of scaled FinFETs by means of multi-million atom modeling (Lansbergen *et al.*, 2008b; Rahman *et al.*, 2009). In this chapter it is shown that the aforementioned technique can be used to perform single donor mapping in advanced Si FinFETs. By carefully examining the fingerprints of isolated donors in an ensemble of devices, the chemical species, concentration, and local field of donors in the channel region can be determined in a non-intrusive fashion.

11.4 Devices

The FinFET devices used in this study consist of crystalline silicon wires (fins) with large contacts patterned by 193 nm optical-lithography and dry etching from silicon-on-insulator (see Fig. 11.1a). After a boron channel implantation, a 100 nm polycrystalline silicon layer was deposited on top of a nitrided oxide (1.4 nm equivalent SiO_2 oxide thickness). A phosphorus (P) implant was used for pre-doping and the structure was subsequently patterned using an oxide hard mask to form a narrow gate. Next, high-angle arsenic (As) implantations were used for source or drain extensions, while the channel was protected by the gate and 50 nm wide nitride spacers and remained p type. Finally, As and P implants and a NiSi metallic silicide were used to complete the source or drain electrodes. The samples described in this chapter all have a gate length of 60 nm.

Transport measurements are performed on an ensemble of devices at a temperature of 4 K and a search for the fingerprints of isolated donors is performed (see previous chapter). These single donors are located in or near the active cross section of the channel, i.e., the cross section of the FET body where the potential is lowest and the electrical transport thus takes place. Large electric fields

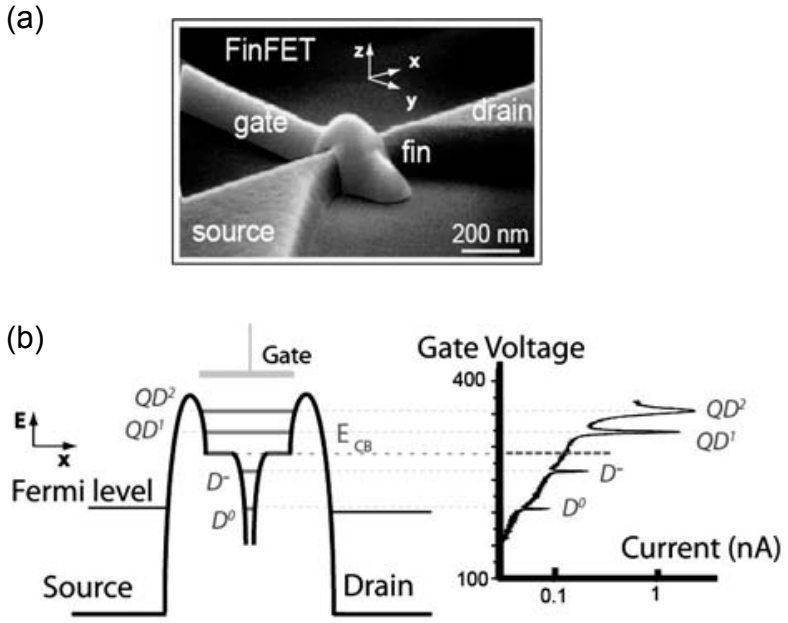

Figure 11.1. Geometry and electrical characteristics of a single donor located in the channel of a FinFET device. (a) Scanning Electron Micrograph of a typical FinFET device. (b) Band diagram along the x-direction with the D^0-state in resonance combined with the measured source/drain current versus gate voltage for a typical sample. QD^1 and QD^2 indicate resonances of a quantum dot, formed by the confinement provided by the corner effect and residual barriers in the access regions between source/drain and channel. The gate voltage where the band edge in the channel is aligned with the Fermi energy E_F in source/drain, indicated by E_{CB}, is estimated by subtracting one unit of addition energy from QD^1. Below the band edge, there are resonances ascribed to the D^0 and D^- charge states of a single donor. © 2008 IEEE. Reprinted, with permission, from Lansbergen, G. P., Rahman, R., Wellard, C. J., Caro, J., Collaert, N., Biesemans, S., Klimeck, G., Hollenberg, L. C. L., and Rogge, S. (2008). Transport-based dopant metrology in advanced finFETS, pp. 1–4, doi:10.1109/IEDM.2008.4796794.

induced by the gate or even corner effects can reduce the active cross section to dimensions much smaller than the FET body (Sellier *et al.*, 2007). Furthermore, as described in the previous chapter, corner effects play a major role in these devices, as indicated by an active cross section of only 4 nm^2, determined by thermionic transport measurements (Sellier *et al.*, 2007).

A single donor's fingerprint is characterized by a pair of resonances in the source–drain current, I_{SD}, versus gate voltage, V_G, characteristics at low V_{SD} (Fig. 11.1b). The positions of a pair of resonances in V_G are an indication of the energy of the one-electron

(D^0) and two electron charge states (D^-). A large quantum dot present in the channel (with charge states indicated by QD^1 and QD^2) is also observed, which allows a rough determination of the position of the band edge in the active area. While the quantum dot in the channel is almost always found, only about one out of seven devices shows the fingerprint of a donors. The identification of the resonances of the donor is based on the determined binding energy, charging energy and the odd-even spin filling (Sellier *et al.*, 2006). Next, the excited energy levels of the one-electron (D^0)-state are determined by sweeping both the V_G and V_{SD} biases and measuring the differential conductance (dI_{SD}/dV_{SD}) in the appropriate bias space see Fig. 11.2. In this so-called stability diagram the typical diamond-shaped region associated with Coulomb-blocked transport between the D^0 and D^- states is observed. The total electronic transport in the conducting regions increases as an excited level of the D^0-state enters the bias window defined by source/drain, giving the stability diagram its characteristic pattern (Sellier *et al.*, 2006, 2007) indicated by the dashed black lines. The red dots indicate the combinations of V_{SD} and V_G where the ground state is at the Fermi energy of the drain and an excited state is at the Fermi energy of the source. It is the bias voltage V_{SD} in this combination that is a direct measure for the energy of the excited state ($eV_{SD,N} = E_N$), where E_N is the energy relative to the ground state and N is the level index). The excited states as determined in this fashion are depicted in Table 11.1. These levels are not bulk-like but heavily influenced by the local electric field and the nearby interface (Smit *et al.*, 2003; Calderón *et al.*, 2006; Rahman *et al.*, 2009).

Finally, the measured level spectrum is compared to a multi-million atom tight-binding NEMO 3-D calculation (Klimeck *et al.*, 2009) of the system taking two possible chemical species, As and P, into account. NEMO 3-D solves for the eigenvalues of the single electron Schrödinger all band equation in a tight-binding approach (Klimeck *et al.*, 2002). The NEMO simulation package is based on about 14 years of development at Texas Instruments, NASA Jet Propulsion Laboratory, and Purdue University (Klimeck *et al.*, 2002, 2009). Each atom is explicitly represented and the electronic structure of the valence electrons is represented by ten $sp^3d^5s^*$ orbitals. Spin can be included explicitly into the basis by doubling the

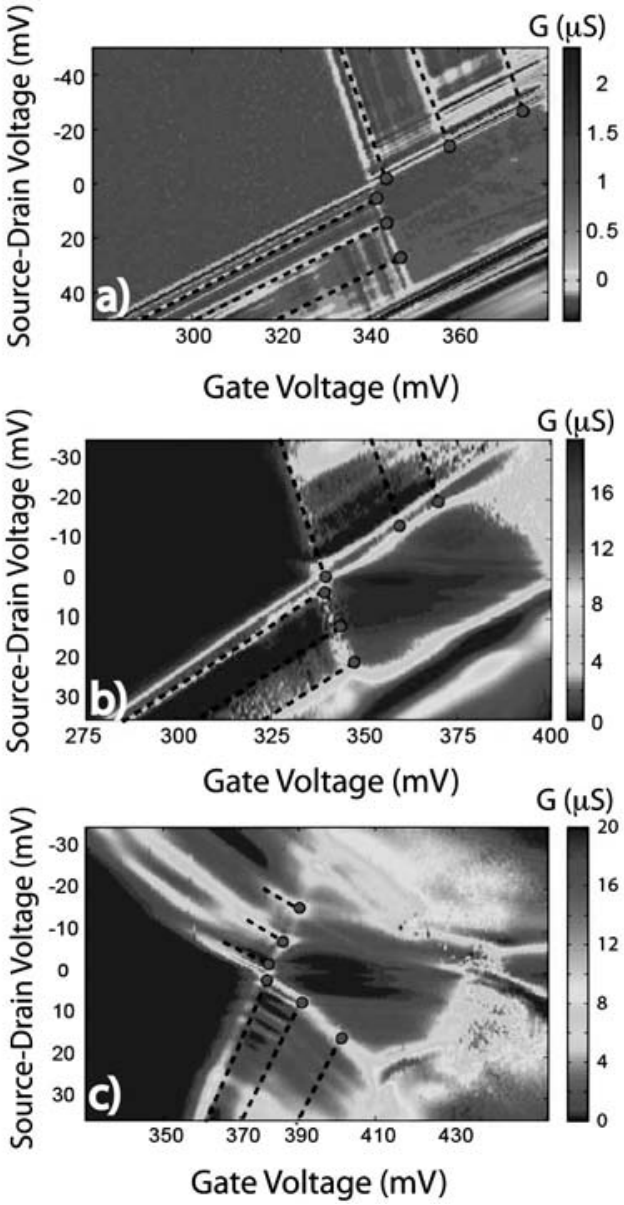

Figure 11.2. Source/drain differential conductance of the D^0 charge state as a function of bias voltage and gate voltage of typical single donor FinFET devices. The excited states, indicated by the black dashed lines, form the fingerprint by which the donor properties can be identified. The dots are a direct indication for the energy of these states ($E_i = eV_{\mathrm{SD}}$, with E_i the i-th excited state and e the unit charge.) (a) Sample 13G14: Excited states are observed at 3.5, 15.5 and 26.4 meV (b) Sample 10G16: Excited states are observed at 2, 15, and 23 meV. (c) Sample GLJ17: Excited states are observed at 2, 7.7, and 15.5 meV. © 2008 IEEE. Reprinted, with permission, from Lansbergen, G. P., Rahman, R., Wellard, C. J., Caro, J., Collaert, N., Biesemans, S., Klimeck, G., Hollenberg, L. C. L., and Rogge, S. (2008). Transport-based dopant metrology in advanced finFETS, pp. 1–4, doi:10.1109/IEDM.2008.4796794.

Table 11.1. First three measured excited states of each sample (see for example Fig. 11.2) versus the best fit to the NEMO 3-D model (as depicted in Fig. 11.3). The fit yields a unique combination of (F, d) for each single donor device. The measurement error for each level is estimated to be around 0.5 meV

Device		E1 (meV)	E2 (meV)	E3 (meV)	d (nm)	F (MV/m)	s (meV)
10G16	Exp	2	15	23			
	TB	2.2	15.6	23.0	3.3	37.3	0.59
11G14	Exp	4.5	13.5	25			
	TB	4.5	13.5	25.0	3.5	31.6	0.04
13G14	Exp	3.5	15.5	26.4			
	TB	3.6	15.7	26.3	3.2	35.4	0.17
HSJ18	Exp	5	10	21.5			
	TB	4.5	9.9	21.8	4.1	26.1	0.63
GLG14	Exp	1.3	10	13.2			
	TB	1.3	10	12.4	5.2	23.1	0.28
GLJ17	Exp	2	7.7	15.5			
	TB	1.3	7.7	15.8	4.9	21.9	0.77

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number of orbitals. Spins are coupled through spin-orbit coupling resulting in accurate valence band states. The five d orbitals help shape the curvature of the conduction bands to achieve appropriate masses and symmetries at X and L. The tight-binding parameters are tuned to reproduce the bulk silicon properties under various strain conditions faithfully. For systems where the primary interest is in the conduction band properties and if no magnetic fields need to be considered, spin can safely be ignored without any significant loss of accuracy. Effects due to crystal symmetry, strain, local disorder, and interfaces can be explicitly included in the model through direct atomic representation.

The single impurity states are modeled with a simple Coulomb potential away from the impurity site and a central on-site core correction to match experimentally observed bulk-like impurity energies. The simulation domain for a bulk-like single impurity must be large enough such that the hard wall boundary conditions imposed by the finite simulation domain are not felt by the central impurity. With a simulation domain of $30.4 \times 30.4 \times 30.4$ nm^3

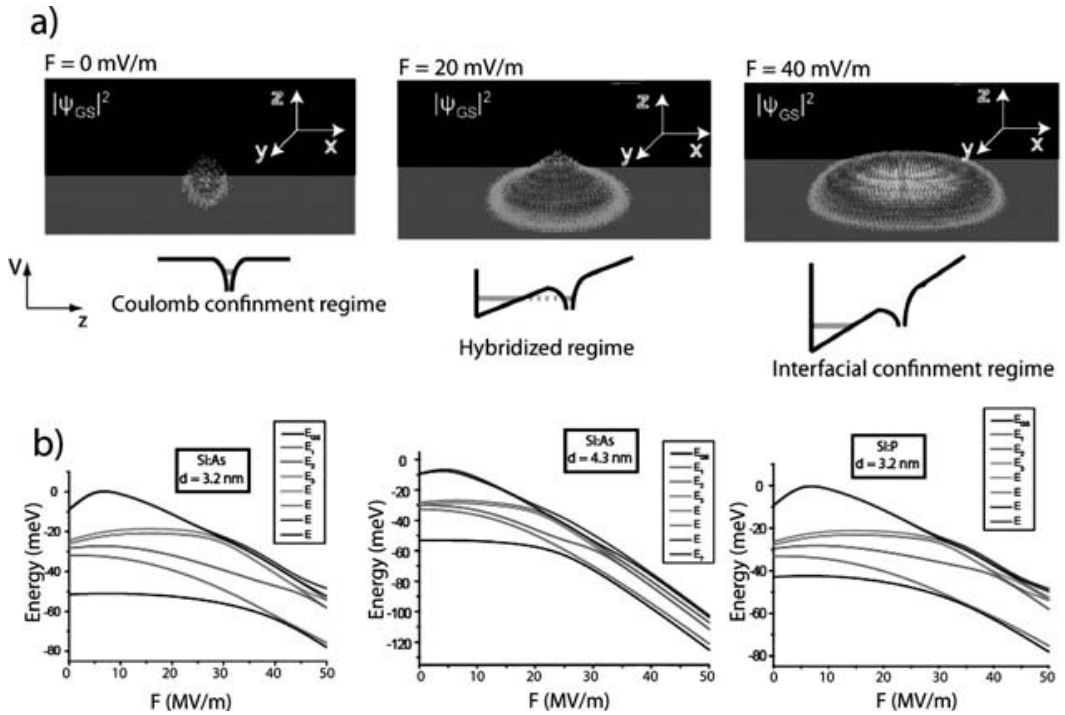

Figure 11.3. (a) Calculated wave-function density of an As donor with $d = 4.3$ nm for three different fields. The gray plane indicates the SiO_2-interface. From low-fields (where the donor has a bulk-like spectrum) to high fields, the donor electron makes a transition from being localized on the donor to being localized at the silicon interface. (b) First eight eigen-levels of an As donor 3.2 and 4.3 nm below the interface and a P donor 3.2 nm below the SiO_2 interface as a function of electric field (F) calculated in a tight-binding model (NEMO 3-D). Note that we measure excited states relative to ground state (lower black line in this graph.) © 2008 IEEE. Reprinted, with permission, from Lansbergen, G. P., Rahman, R., Wellard, C. J., Caro, J., Collaert, N., Biesemans, S., Klimeck, G., Hollenberg, L. C. L., and Rogge, S. (2008). Transport-based dopant metrology in advanced finFETS, pp. 1–4, doi:10.1109/IEDM.2008.4796794. See also Color Insert.

corresponding to about 1.4 million silicon atoms the impurity eigenstates move less than 1 μeV with further domain size increases. A critical modeling capability here is the need to be able to compute reliably the ground states as well as the excited states of the impurity system, as that is a significant component of the impurity fingerprint. Figure 11.3b shows typical eigenstate spectra for an As donor (two donor depths) and a P donor as a function of electric field. Three electric field regimes can be distinguished (Fig. 11.3a). At the low field limit ($F \sim 0$ mV/m) the spectrum of a bulk As donor is obtained. In the high field limit ($F \sim 40$ MV/m) the electron is pulled into a triangular well formed at the interface and the donor is ionized (Smit *et al.*, 2003; Calderón *et al.*, 2006; Lansbergen *et al.*, 2008b). In the cross-over regime ($F \sim 20$ MV/m) the electron is de-localized over the donor- and triangular well potential and the level spectrum consists of levels associated with the donors, levels associated with the triangular well at the gate interface (formed by the local field) and hybridized combinations of the two (Calderón *et al.*, 2006; Lansbergen *et al.*, 2008b; Rahman *et al.*, 2009).

The measured level spectra are least-square fitted to a calculation over a sufficiently sized region of F–d (field and donor depth parameter space). At least three excited levels per donor are taken into account to make the fit over-determined. The fitting procedure is performed for two different species of donor atoms, As and P, which were both used in the fabrication process. The concentration of donors in or near the active area of the FET channel can be estimated by comparing how many times a single donor is identified with the relevant volume where donors can be found.

11.5 Results

Of the 42 devices that have been examined, six have been found to exhibit the fingerprint of a single donor in the transport characteristics. These devices were subsequently measured carefully and the D^0 level spectrum was fitted. The quality of the fits, indicated by $\chi 2$, across the six samples is 0.92 ($\chi 2 < 1$ means a good fit) assuming As donors. For P donors, we find a $\chi 2$ of 10.22 (although two of the six are comparable in quality.) Based on the fits, the donors active in the devices are assumed to be As. The (over-determined)

fit furthermore yields a unique combination of (F, d) for each single donor device, as shown in Table 11.1, together with the measured level spectra, and their fits.

Finally, it is also possible to obtain the donor concentration. As mentioned before, the active cross section of the devices are heavily reduced by a corner effect (Sellier *et al.*, 2007). The identified donors are either in or near these corners, and from the least-square fit we actually know the donor depths range from $\sim$3 to 6 nm below the Si/SiO_2 interface, see Table 11.1. The part of the FinFET channel where donors are found is a volume spanned by the donor depths and the gate length (60 nm), and a single donor device is found in average only in one out of seven devices that are measured. This means that for each $\sim$1000 nm^3 of measured material it is possible to found one As dopant, and, as a consequence, a local As concentration of about 10^{18} cm^{-3} can be extrapolated.

11.6 Conclusions

In this chapter a novel method for dopant metrology is introduced. The excellent quantitative agreement between the measured and modeled level spectra gives an indication of the high level of confidence of this method to determine the chemical species and local field of single impurities in silicon FinFET transistors. Furthermore, the local concentration of donors near the active cross section of the FinFET can be estimated. The present method offers opportunities for non-invasive characterisation down to the level of a single donor and could be a future tool in the guidance of device processing. This is especially true for such CMOS devices for which variability problems are increasing dramatically with ultra-scaling and this justifies the importance of the method described here.

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